ABSTRACT

LOVELACE, WILLIAM MATHIESON. Multi-User Performance Issues in Wireless Impulse Radio Networks (Under the direction of Professor Keith J. Townsend).

There has been a growing interest in Ultra Wide Band (UWB) communication technologies over the last ten years. Motivated by advances in narrow pulse generation techniques and the potential for VLSI digital receivers, much fundamental research has been devoted to UWB. Most of the research to date has been dedicated to the potential for dense multi-user environments, narrow band interference issues, and multi-path considerations.

While Impulse Radio (IR) has shown tremendous potential for high throughput local area networks based on time domain separation techniques, the stringent parametric assumptions required for practical implementation have not been clearly evaluated. Specifically, two of the more common constraints required to meet the projected UWB performance measures are timing tolerances and multi-user interference control. The work here has addressed both of these critical issues.

Our work is the first to quantify the effects of timing jitter and tracking on time-hopping UWB multi-user performance. The investigations of these issues show that the performance of binary and 4-ary impulse radio is very sensitive to timing jitter and tracking errors. Supported multi-user performance is quantified through simulation and finds orthogonal pulse position modulation (PPM) out performed binary offset PPM at all jitter levels in thermal and pulse noise. We also compare accepted narrowband tracking techniques to an efficient error tracking method adapted to UWB.

With adequate understanding of the effects of timing jitter an IR receiver can be designed to meet a given performance. However, the control of local user power for a given receiver is not always guaranteed in practical environments or under complete control of the receiver. A typical spread-spectrum IR that employs a matched filter sum for bit decisions is susceptible to small numbers of large power pulses that can dominate the bit decision statistics. We propose a simple chip discrimination technique for use with UWB that improves performance for large near/far interference ratios. The technique exploits the unique time domain characteristics that only UWB systems can provide by applying individual chip discrimination prior to the spreading summation. A statistical model is devel-

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oped that predicts bit error performance for binary offset pulse position modulation (PPM) as a function of near/far density and power for varying discrimination thresholds. We find that even a small number of very near interferers can greatly reduce the performance of a system without blanking or discrimination. Results show substantial improvement using our method for near interferers with near/far power ratios greater than 20 dB.

By further adapting the chip discrimination method to the dynamics of a bursty packet network, we derive a technique for adjusting the number of chips per bit to maximize throughput of a transmission queue. Leveraging the information derived from the chip discrimination approach, as a component to a peer-to-peer MAC layer protocol, we can affect more efficient transmission rate control. The combination of these two techniques greatly improves performance in poor near-far power ratios and out performs fixed parameter links. The efficiency of this method is demonstrated using simulation in bursty, pulse limited environments and compared to equivalent $M|D|1$ queue statistics as a benchmark.

Theoretical solutions for perfect blanking cases are derived to support simulation results and provide parametric optimization tools. Adaptation of these methods are applied to a simple ALOHA packet network to illustrate the effectiveness of chip discrimination and rate control to overall network throughput.

Multi-User Performance Issues in Wireless Impulse Radio Networks

by

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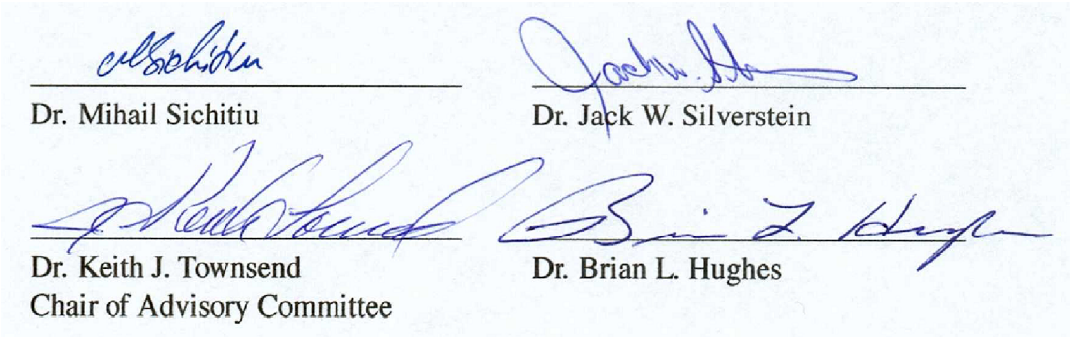

To the support and encouragement from Susanne and Natalie

Biography

William Lovelace received the B.S. degree in Electrical Engineering from Rensselear Polytechnic Institute in 1980 and his M.S. in Electrical Engineering from the University of Florida in 1982 with Dr. Leon Couch. He then joined Eurotel Ltd. in Weybridge England developing drop and insert multiplexers for terrestrial data links. From 1987 to 1994 he worked with TRW's Military and Electronics Division developing integrated avionics systems for advanced tactical aircraft. This work required the adaptation of a wide variety of requirements from several communication systems including SINCGARS, HAVEQUICK, JTIDS, IFF and other classified links. He also provided key system engineering support for the successful flight demonstration on YF-22 resulting in the award of the integrated communication avionics suite on F-22.

In 1994 he joined Ericsson's Land Mobile Systems and cellular group in Raleigh NC as principal system engineer directing air interface designs and evaluating link performance requirements. There he successfully developed and demonstrated Ericsson's introduction of digital modulation technologies required to meet stringent performance and spectral constraints of the land mobile radio emergency services market. In the cellular group he was a lead system engineer for the development and approval of Ericsson's introductory cellular handset into the Japanese market. This position required oversight of design performance issues and addressed the novel diversity receiver requirements. Additionally he participated in the development of other critical technologies such as *Bluetooth*© as an internal consulting system engineer.

Currently he is completing a Ph.D. with Dr. Townsend in Electrical Engineering at North Carolina State University. His Ph.D. research interest is in the novel area of ultra-wideband communications networks addressing fundamental issues limiting the anticipated performance of UWB links. Other research interests include modeling, simulation and analysis of telecommunication systems. Bill is a member of Eta Kappa Nu and a member of IEEE for 20 years.

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I would especially like to thank my advisor Dr. Keith Townsend for for seeing the potential and taking on the uncertainty of a more mature student. His thoughtful guidance and encouragement has inspired me throughout this effort. The many hours of collaboration and insightful comments have added greatly to this research. I also wish to thank my committee members, Prof. Brian Hughes, Prof. Michail Sichitiu and Prof. Jack Silverstein for their helpful comments and feedback throughout the examinations as well as their keen interest in this novel research topic. Many thanks also go to Dr. Robert Ulman of the Army Research Office (ARO) for his interest and collaboration on this research. The ARO has provided encouragement and continued support under contracts DAAD19-00-1-004 and DAAG55-98-D-0003.

I especially thank my parents for their never-ending patience in a seemingly endless desire for further education. It seems to never end.

Above all, I would like to particularly thank my wife Susanne for her unwavering encouragement and motivation throughout this mid-career aspiration. Without her selfless support and understanding this truly would not have been possible. I also wish to thank my daughter Natalie for teaching me lessons far more important than any discipline of higher education and showing patience beyond her age.

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Chapter 1

Introduction: Critical UWB Performance Issues

Wideband pulse position modulation techniques have been around for most of the last century. However technology advances in very narrow pulse generation and the pressure on spectrum for high throughput local networks have recently stimulated research into ultra-wideband (UWB) time domain based communication systems. The advantages of such an Impulse Radio (IR) [3] concept have shown tremendous potential for dense muti-user environments [4, 5] with significant throughput. The trade off between frequency and time selectivity results in the potential for a receiver of very low front end complexity leveraging advances in high-speed digital logic for time domain discrimination. The reduction or elimination of frequency selective elements also results in potentially smaller transceivers. The resulting low duty cycle of a sub-nanosecond Impulse Radio also suggests overall transponder power budget savings. With the added market advances in local wireless networks and the pressure for spectrum allocation much interest has been promoted for IR as a local high throughput multi-user solution.

Much of the initial theoretical research in IR has focused on multi-user capacity, pulse position modulation options and techniques in resolving signals in a dense multi-path en-

vironment [6, 7, 8, 9]. Most of these results have come with some crucial assumptions regarding timing resolution and power control. The fundamental tradeoff in the reduction in frequency selectivity comes back as a stringent time domain constraint. Sub-nanosecond pulses inherently place tight tolerances and resolution on the time domain. Even the unrealistic multi-user equal power assumptions threaten to limit much of the gains attributed to Impulse radio in a practical environment. The work here has contributed to the understanding of these limitations and has provided solutions to some of these problematic assumptions.

1.1 Clock Tolerance

The potential advantages of an IR system of sub nanosecond pulse dimensions have been well highlighted. Multiple pulse per bit modulation with power spread over a broad spectrum, potentially limiting interference to conventional frequency selective systems, has been studied and even prompted the Federal Communications Commission (FCC) to allow limited testing within broad spectral envelopes. Even tactical systems can be envisioned that leverage the spread spectrum capabilities of IR for low duty cycle covert applications. Most of the theoretical expectations for IR have implicitly assumed that peer-to-peer links have exact knowledge of transmitter pulse sequence timing. What has not been well documented is exactly how critical timing errors are to an IR system with chip pulses on the order of a nanosecond.

Early commercial development has certainly begun to realize the importance and complexity of a time base for IR [10, 11, 12]. Tracking and offset errors in IR may seem obviously critical but even more ubiquitous clock parameters such as short-term jitter can be quite a problem. However the potential multiuser performance anticipated by IR had not been well quantified for timing jitter in the literature until we illustrated the problem in [13, 14]. This work is also described in Chapter 2 for timing jitter and tracking errors. Our results show significant performance degradation unless jitter variances are maintained within 10 ps RMS. Traditional narrow band early-late gate tracking methods are also evaluated here illustrating another significant source of error.

Since our work a number of researchers have developed jitter measurement techniques [15] and described performance issues associated with clock jitter [16]. Recent reviews of current research in UWB [17] have identified our work as one of the key issues for UWB. Specific extensions of this research from [18, 19, 20, 21] have furthered theoretical development of this critical timing issue. It's now clear that practical expectations for IR must be designed with timing tolerances in mind. Future work in this area will include pulse modulation techniques and tracking methods that can provide robust performance within reasonable clock performance parameters.

1.2 Near Far Power

Most practical wireless networks must contend with the dynamic range discrepancy of the near-far power problem. The literature is replete with research and techniques to deal with near-far power issues associated with contemporary CDMA and frequency selective networks [22, 23, 24]. Frequency channel assignment or coordinated methods of orthogonal resource allocation have been used to mitigate the problem. Some of these methods can yield rather complex MAC layer protocols and overheads on the system. Perfect orthogonal separation is not always possible due to resource limitations or environmental conditions. An overview of contemporary MAC layer techniques can be found in the associated JSAC papers in [25].

Impulse radio is no different in this respect and is also very susceptible to power discrepancies between near and far transponders. Although much research can be advanced with equal power assumptions the practical issue of mutual interference must be considered. Several methods have been applied to IR recently to address near-far power issues. Under some conditions of reasonable multi-path, control of orthogonal hopping codes [26] have been suggested. Longer codes used to provide better separation can be used but at the expense of data rates. The effectiveness of power control [27] depends on the geometry of the network and require reliable feedback of receive power. One advantage that IR can apply to power control [28] is the inherent ranging information associated with a fine time oriented system to select appropriate power levels. Other more complex techniques employ

full multi-user detection to effectively null signals from all users except the desired signal [28]. Practically though, tracking all users with a high degree of timing resolution in a dynamic environment with multiple reflections requires a high level of receiver complexity. It cannot even be assumed in tactical systems that all nodes would be cooperative in power control or code selection [29].

The effects of unequal power have been quantified in [30] and the relative performance loss of using a hard limiter as an alternative to overcoming unequal power are shown in [31]. Several papers have proposed complex MAC layer networks [32, 33] to control resources in IR to mitigate the problem. Unfortunately simply porting MAC layer techniques derived from narrow band systems [34, 35] does not take advantage of unique characteristics of IR, or worse, erroneously assumes equivalent characteristics.

In contrast to the complexity of MAC layer based power control methods, the technique described in Chapter 3 leverages the unique characteristics of IR. By constraining the network to the assumption of autonomous or uncoordinated nodes and working with the low pulse duty cycle nature of impulse radio, a very simple first order method for mitigation of multi-user interference has been proposed [36, 37]. Unlike other methods presented, individual Chip Discrimination uses only locally derived receiver information and does not require complex timing acquisition of local interferers. Not only does such a method have advantages in hostile uncooperative tactical environments but also in commercial indoor environments where very near co-site placement and dense multi-path may occur.

1.2.1 Rate Control

Nearly all previous work has assumed static spreading rates for IR links or has implemented relatively slow rate control using complex interfering power estimation. Fixed rate methods place either strict assumptions on the environment or select rates for worst case events that may occur infrequently. MAC layer intensive rate control methods proposed so far [34, 35] are well known narrow band solutions overlaid on an IR network and unoptimized for unique IR characteristics. Both these methods remain relatively inefficient in potentially bursty or uncooperative environments.

The unique pulse interference estimation technique used for near-far power adaptation in Chapter 3 has been further modified for rate control optimization in bursty network environments and shown [38] to provide improved throughput efficiency. Unlike previous work, this method described in Chapter 4 uses self-derived pulse environment statistics to select a timely spreading rate for the transmitter. Since the same environment estimation logic is used for both near-far power adaptation and rate control, the added complexity is limited to communication of the rate selection from peer-to-peer. The combination of chip discrimination in Chapter 3 and rate adaptation from Chapter 4 both take advantage of the unique low duty cycle characteristic of IR not available in other narrow band methods.

1.2.2 Discriminating Techniques Applied to Packet Performance

Chapters 3 and 4 show how chip (pulse) discrimination can be used to adapt a UWB chip per bit rate to optimize throughput under conditions of large near-far power ratios. Chapter 5 takes advantage of these techniques to develop a theoretical basis for packet transmission success using adaptive chipping (spreading) rates under harsh near-far power ratio environments. The effects on IR packet performance can be enhanced by leveraging the low duty cycle characteristic of impulse radio to mitigate the effects of large interferers. Straightforward coordinated blanking methods often require the acquisition and tracking of potentially many local interferers. Unlike these complex methods, the technique used in this packet implementation uses only locally derived receiver information for interfering pulse blanking and chip/bit rate selection. Even if the complexity of tracking multiple sources could be afforded [39], the dynamic and close quarter environments of tactical battlefield situations prohibit the assumption that all nodes are cooperative in power control or code selection. Networks in this environment would clearly benefit from the autonomous approach to blanking and throughput optimization developed here. The theoretical algorithm developed in Chapter 5 along with simulation can be used as a tool to rapidly evaluate the effects of IR design parameters. Parameter and rate adaptation can be optimized for given harsh interfering cases. Once more we show the advantage of adaptive rate control in harsh interfering environments resulting in more efficient throughput to that of fixed rate

methods. Theoretical results are in good agreement with simulation runs of peer-to-peer links with high throughput and bursty interference.

The theory developed in Chapter 5 ascertained the effects of chip discrimination and rate control for a peer-to-peer packet link for a given interfering environment. Chapter 6 takes this a step further to better explain the overall network capacity effects. This is done by applying techniques recently developed for CDMA networks [40] and adapting them to fit IR. Continuing with the emphasis on reduced coordination complexity in IR we consider a fundamental ALOHA packet network similar to those considered for CDMA [41]. Given the theoretically large multi user densities supported with equal power assumptions, the capacity of an IR ALOHA network would also be expected to be quite large under the same assumptions. However, as noted throughout this development, IR performance is very susceptible to strong interferers and power inequality. Chapter 6 considers ALOHA network capacity with assumed strong pulse interference and perfect blanking. The theory applied to packet interference in this case uses a Markov process to derive the overlap packet expectations. Results are consistent with packet losses found in Chapter 5 and simulations of the network.

As before, we consider the effects of blanking and rate control, but apply these methods to all transmitted packets in the environment as a rule. The selection of the chip per bit rate and frame time is shown to have a significant effect on the overall capacity of the system. Throughput of a fixed data size packet is optimized for these parameters. The performance and parameter optimizations are compared for receiver implementations of a hard limited pulse receiver to that of a pulse discriminating receiver. The IR adaptive rate tables developed for this environment show performance characteristics much like the Channel Load Sense Protocols (CLSP) do for traditional ALOHA packet systems. We show how it's possible to meet the optimum CLSP capacity performance for the best fixed rate IR network but with a significant overall reduction in pulse density by using adaptive techniques developed in Chapter 4. The passive techniques of chip discrimination and simple rate selection have been applied to packet transmission resulting in optimum capacities with a significant reduction the required power.

Chapter 2

Timing Tolerance

2.1 Clock Jitter

Impulse radio (IR) has shown the potential for dramatic throughput in high multi-user environments leveraging the ultra-wideband nature of sub-nanosecond pulses [4, 5]. Many of the IR attributes hold promise for tactical systems where low power covert operation is desirable. Such covert systems deployed in a standalone peer-to-peer network may take advantage of the low power and duty cycle of IR to provide modest throughputs with very low power spectral densities [42, 43]. While extremely high multi-user densities are possible with IR, the tactical application may require leveraging potential system bandwidth for covert power levels and overall low power consumption. Many considerations apply to the design of such standalone covert IR systems such as assumed pulse densities, peak and average pulse power levels and complexity.

Impulse radio has been analyzed under a number of conditions including equal power multi-user environments with binary signaling [4, 5], M-ary signaling [6], and dense multipath [9]. Medium access control (MAC) layer issues such as power control and peer-to-peer architectures specific to issues related to a covert impulse radio network have been investigated [27, 44, 31].

One issue important to IR that has not been considered in the literature and requires a serious design budget consideration is timing tolerances. The reduced complexity and other implementation advantages offered by IR in terms of filtering and linearity are somewhat offset by more stringent timing tolerances. This chapter describes the effects of timing jitter and tracking errors on the performance of IR. The implications of timing errors on IR performance are more pronounced since IR is based on the transmission of very narrow pulses. Only recently have clocks with reasonable stability and lower power consumption suitable for UWB systems been reported [10]. The jitter reported in [10] is on the order of 10 ps, and clock stability is only one component of the total system jitter budget. Even with very stable clocks, there are other contributions to the total jitter budget including tracking and relative velocities between transmitter and receiver.

Results of simulations for binary and 4-ary signaling illustrate the sensitivity of IR to timing errors. Overall throughput degradation and design considerations associated with these errors are considered. The eventual throughput, power budget and complexity for an IR system are closely coupled to clock stability and tracking. The tradeoff between binary and 4-ary signaling in the presence of timing errors show that 4-ary signaling outperforms binary signaling over a wide range of operating parameter values.

Another important source of timing jitter illustrated in this chapter is tracking error [1, 45, 46]. Even without clock jitter at the sources, the noise introduced at the timing tracker jitter the sample timing. The MAC layer of a peer-to-peer network must track and maintain relative drift rates of each link and offset the receiver clock. Even with ideal compensation for drifting clocks, random uncoordinated pulse arrivals contribute interference noise to the filtered tracker causing jitter on the receiver window.

This chapter is organized as follows. In Section 2.1.1, we present the model of the UWB system considered. The model includes timing jitter and an early-late gate tracker. Simulation results showing the performance of binary and 4-ary UWB systems with timing jitter and tracking are given in Section 2.1.2. Concluding remarks are provided in Section 2.3.

2.1.1 System Model

Binary Signaling

In the CDMA approach for impulse radio used in [4, 44, 27] the transmitted signal is a periodic pulse train with a low duty cycle consisting of pulses of approximately 1 ns in duration. The pulses are further dithered based on the pseudorandom code (PN) sequence, where each user employs a different offset. A summary of the basic transmission system is described here [4, 44, 27] with the modifications required for pulse timing jitter.

Consider a time-hopping signal transmitted from the j^{th} transmitter, $s^{(j)}(t)$, given by

$$s^{(j)}(t) = \sum_n p\left(t - nT_f - h_n^{(j)}T_h - \delta d^{(j)}_{\lfloor n/N_s \rfloor} + \varepsilon_n^t\right) \tag{2.1}$$

where $p(t)$ is the monocycle pulse waveform, T_f is the average time between two pulses (frame time), $h_n^{(j)}$ is a pseudorandom code sequence unique to transmitter j, T_h is the discrete time shift added to the pulse depending on the code sequence such that the total time-hopping shift is given by $h_n^{(j)}T_h$, and N_s is the number of pulses per information bit. The addition of timing jitter for the transmitter is given by a zero mean normally distributed random variable ε_n^t, which accounts for the timing uncertainty for the n^{th} transmitted chip. Each information bit from the binary sequence, $d^{(j)}_{\lfloor n/N_s \rfloor}$, is encoded in the pulse train by delaying N_s monopulses by an additional amount, which can be written as

$$\text{Delay} = \begin{cases} 0 & \text{if } d^{(j)}_{\lfloor n/N_s \rfloor} = 0 \\ \delta & \text{if } d^{(j)}_{\lfloor n/N_s \rfloor} = 1 \end{cases} \tag{2.2}$$

Detection of the transmitted bits is achieved by correlating the received signal with a template signal for a single bit duration in the binary case. The received signal, $r(t)$, is given by

$$r(t) = \sum_j^{N_u} \alpha_j s^{(j)}(t - \tau_j) + n(t) \tag{2.3}$$

where N_u represents the number of users in a multiple access channel, α_j is the gain of the j^{th} user, τ_j the random time variable representing the asynchronous relationship between user j and the desired signal, and $n(t)$ the Gaussian thermal noise. In all cases studied here the attenuation term $\alpha_j = \alpha : \forall j$. For the binary receiver the template waveform used in the correlator for the q^{th} bit, $v(t)$, is formed by the difference between two waveforms,

$$v_{bit}(t) = p_{bit}(t) - p_{bit}(t - \delta) \tag{2.4}$$

where $p_{bit}(t)$ is given by

$$p_{bit}(t) = \sum_{n=qN_{si}}^{(q+1)N_{si}-1} p\left(t - nT_f - h_n^{(i)} T_h + \varepsilon_n^r\right) \tag{2.5}$$

We assume that the receiver is selecting the i^{th} desired transmitter and that $\tau_i = 0$ for this case. As was the case for the transmitter, the receiver clock for p_{bit} is modified for timing error with the independent random variable ε_n^r. Again this error is modeled as a zero mean normally distributed random variable. The binary bit decision for the q^{th} data bit made at the correlator output is given by

$$\text{Decide } d_q^{(i)} = \begin{cases} 0 & \text{if } \int_{t\in\{\mathcal{B}_q\}} r(t) v_{bit}(t) dt > 0 \\ 1 & \text{if } \int_{t\in\{\mathcal{B}_q\}} r(t) v_{bit}(t) dt \leq 0 \end{cases} \tag{2.6}$$

where $\{\mathcal{B}_q\}$ is the set of disjoint time intervals corresponding to the q^{th} bit. Received pulses from other users, thermal noise and timing jitter degrade the detection process.

M-ary Orthogonal Signaling

As a comparison, an orthogonal M-ary signaling is also used. Consider a time-hopping signal transmitted from the j^{th} transmitter, $s^{(j)}(t)$, now given by

$$s^{(j)}(t) = \sum_n p\left(t - nT_f - h_n^{(j)}T_h - \delta M^{(j)}_{\lfloor n/N_s \rfloor} + \varepsilon_n^t\right) \tag{2.7}$$

where $p(t)$ is the monocycle pulse waveform, T_f is the average time between two symbols, $h_n^{(j)}$ is a pseudorandom code sequence unique to transmitter (j). T_h is the discrete time shift added to the symbol depending on the code sequence such that the total time-hopping shift is given by $h_n^{(j)}T_h$, and N_s is the number of pulses per symbol. The addition of a timing jitter for the transmitter is given by a zero mean normally distributed random variable ε_n^t. Each symbol from the M-ary sequence, $M^{(j)}_{\lfloor n/N_s \rfloor}$, is encoded in the pulse train by delaying each of the N_s monopulses by a delay given by

$$\text{Delay} = \begin{cases} 0 & \text{if } M^{(j)}_{\lfloor n/N_s \rfloor} = 0 \\ 1\delta & \text{if } M^{(j)}_{\lfloor n/N_s \rfloor} = 1 \\ 2\delta & \text{if } M^{(j)}_{\lfloor n/N_s \rfloor} = 2 \\ \vdots & \vdots \\ n\delta & \text{if } M^{(j)}_{\lfloor n/N_s \rfloor} = n \end{cases} \tag{2.8}$$

where δ is sufficiently large such that the symbols are orthogonal. Although the symbol positions are sequential in time as selected by $M^{(j)}_{\lfloor n/N_s \rfloor}$, the actual implementation could arbitrarily randomize symbol offsets in the frame or even on a frame-by-frame basis. It is sufficient for our analysis here to consider this case assuming all interfering users are independent in data and pseudorandom spreading.

Detection of the transmitted symbol is accomplished by correlating the received signal with M template signals for a single symbol duration. As in the binary case the received signal, $r(t)$, is given by (2.3). For the M-ary orthogonal receiver, the template waveform

used in each correlator for the q^{th} symbol, $v_M(t)$ is simply the chip impulse response.

$$v_M(t) = p_M(t - \delta_M) \tag{2.9}$$

where δ_M is the delay for the M^{th} symbol relative to the hopping sequence and $p_M(t)$ is given by

$$p_M(t) = \sum_{n=qN_{si}}^{(q+1)N_{si}-1} p\left(t - nT_f - h_n^{(q)} T_h + \varepsilon_n^r\right) \tag{2.10}$$

for each of the symbol correlators. As in the binary case we assume that the receiver is selecting the i^{th} desired transmitter and that $\tau_i = 0$ for this case. As was the case for the transmitter, the receiver clock for p_M has been modified for timing error with the independent random variable ε_n^r.

The M-ary symbol decision for the q^{th} symbol made at the output of the bank of M correlators is made by selecting the largest of the M correlator outputs

$$\text{Decide } M_q^{(i)} = \begin{cases} 0 & \text{if } \int_{t\in\{\mathcal{B}_q\}} r(t)v_0(t)\,dt > \int_{t\in\{\mathcal{B}_q\}} r(t)v_i(t)\,dt : \forall i \neq 0 \\ 1 & \text{if } \int_{t\in\{\mathcal{B}_q\}} r(t)v_1(t)\,dt > \int_{t\in\{\mathcal{B}_q\}} r(t)v_i(t)\,dt : \forall i \neq 1 \\ 2 & \text{if } \int_{t\in\{\mathcal{B}_q\}} r(t)v_2(t)\,dt > \int_{t\in\{\mathcal{B}_q\}} r(t)v_i(t)\,dt : \forall i \neq 2 \\ \vdots & \qquad\qquad\qquad\qquad \vdots \\ M & \text{if } \int_{t\in\{\mathcal{B}_q\}} r(t)v_M(t)\,dt > \int_{t\in\{\mathcal{B}_q\}} r(t)v_i(t)\,dt : \forall i \neq M \end{cases} \tag{2.11}$$

where $\{\mathcal{B}_q\}$ represents the set of disjoint time intervals corresponding to the q^{th} symbol.

2.1.2 Supported Multiple Access Performance

To illustrate the multiple access performance degradation due to timing jitter a specific system simulation was developed. The received impulse $p(t)$ used is defined as

$$p(t) = \left[1 - 4\pi\left(\frac{t}{t_n}\right)^2\right] e^{-2\pi\left[\frac{t}{t_n}\right]^2} \tag{2.12}$$

where t_n= 0.29 ns satisfying the relation $\int_{-\infty}^{\infty} p(t)\,dt = 0$ and is plotted in Fig. 2.1 to illustrate the narrow sample period [4, 5]. The hopping times $h_n^{(j)} T_h \forall j$ are assumed to be independent, identically distributed random variables, uniformly distributed over the frame with the pseudorandom hopping sequence length much larger than N_s. The asynchronous interferers transmission time offset $(\tau_1 - \tau_j)$, for $2 \leq j \leq N_u$ relative to the desired signal are independent, identically distributed random variables, uniformly distributed over [0,T_f].

The system model defines two jitter terms, each associated with the clock jitter at the transmitter and receiver ends of the link. Without loss of generality, the simulation model used sets the total link jitter with the transmitter term ε^t relative to a stationary receiver (i.e., $\varepsilon^r = 0$). When a tracking component is included with the simulation model, the link jitter is distributed between the receiver and transmitter.

For the given results, the frame interval is T_f= 128 ns and the chipping rate is N_s= 100 chips/bit for both the binary and orthogonal 4-ary signaling, where the offset between symbol periods for $\rho > 1$ ns in the 4-ary case. In all cases the bit error rate is equal to 10^{-3} with relative powers set to the sensitivity of the binary signaling case in AGWN only.

Interference Limited Case

Using the model described in Section 2.1.1 and equivalent techniques seen in [4, 44, 27] the maximum number of simultaneous users supported at a 10^{-3} bit error rate is determined. This environment is initially assumed to be interference limited with all users of equal power. One advantage of UWB afforded by the very narrow pulse and resulting narrow correlation window provides reduced potential to pulse-on-pulse interference. The

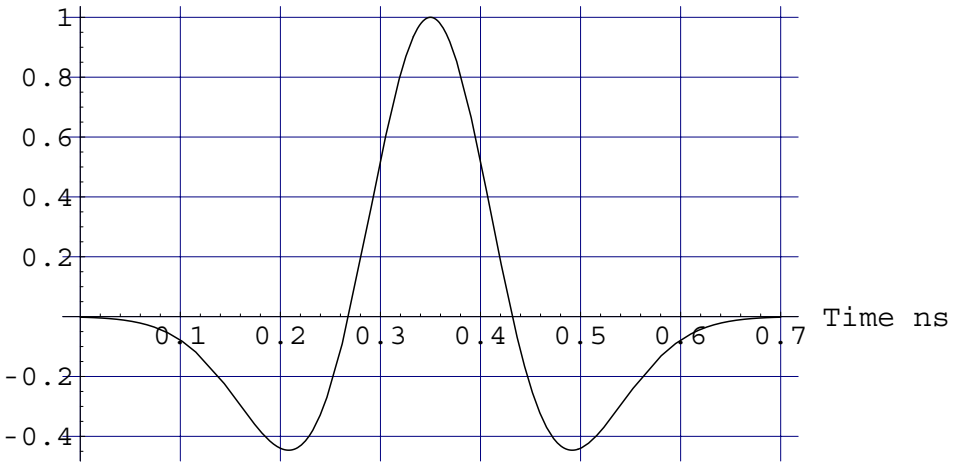

Figure 2.1: Normalized received impulse model response for $t_n = 0.29$ ns.

maximum signal to noise ratio (SNR) is achieved when the correlation receiver is sampled at the peak of the chip. However, unlike some narrowband signaling where the optimum sample period may be relatively flat over a portion of the symbol period, the narrow pulses in the UWB system provide little margin for timing error, as seen in Fig. 2.1.

We evaluate the sensitivity of offset binary UWB signaling [5, 4] by adding a normally distributed sample timing jitter to the matched correlator. The degradation in number of supported users as a function of RMS timing jitter is shown in Fig. 2.2. The decline in performance is quite marked with as little as 30 ps of jitter. Depending on the expected performance of a UWB system a budget for end-to-end timing error must be carefully considered. With a modest 10 ps RMS jitter [10] at the receiver and transmitter and assuming a 10 ps tracking jitter, an end-to-end link jitter of 30 ps reduces capacity from 6650 users to 4700. Even this 30% reduction in peak capacity comes with at least devoting 1/2 Watt of transponder power to maintaining the clock [10]. MAC layer requirements for link maintenance [27] necessitate reacquisition time or power consumption penalties. Unlike narrowband systems where frequency discrimination and linearity are the price for performance, UWB's dual constraint is in the time domain.

In some standalone tactical systems, UWB is considered for its low average transmit power. However, this power savings could be lost if much of the system power is directed to clock stability and compensation. It is possible to recover some of the system throughput

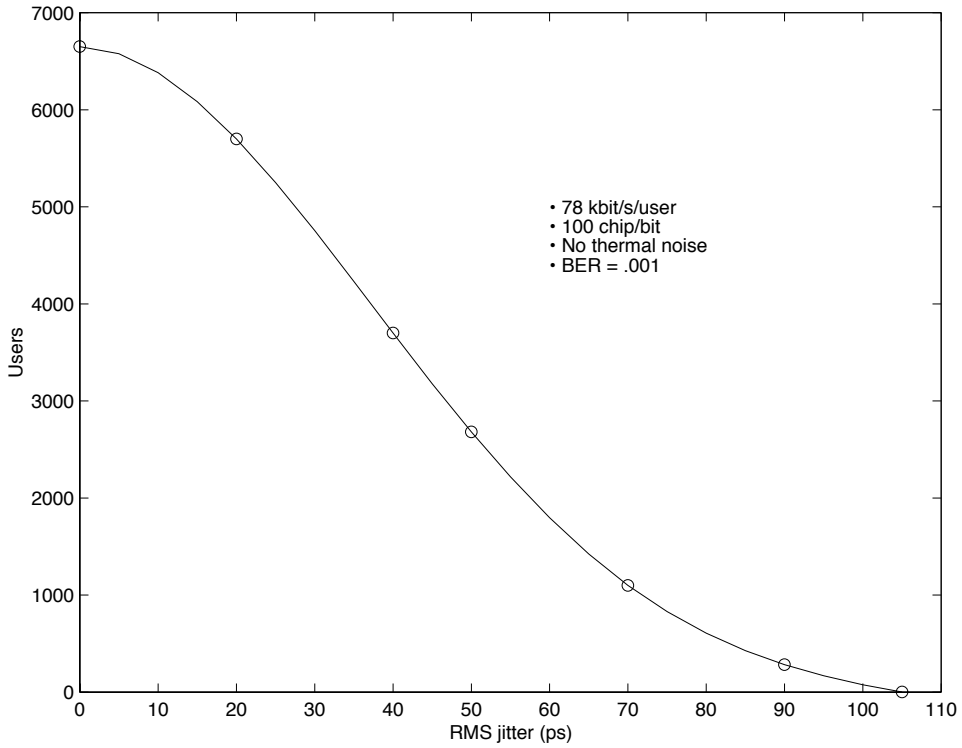

Figure 2.2: Maximum number of users supported as a function of clock jitter for binary antipodal signaling.

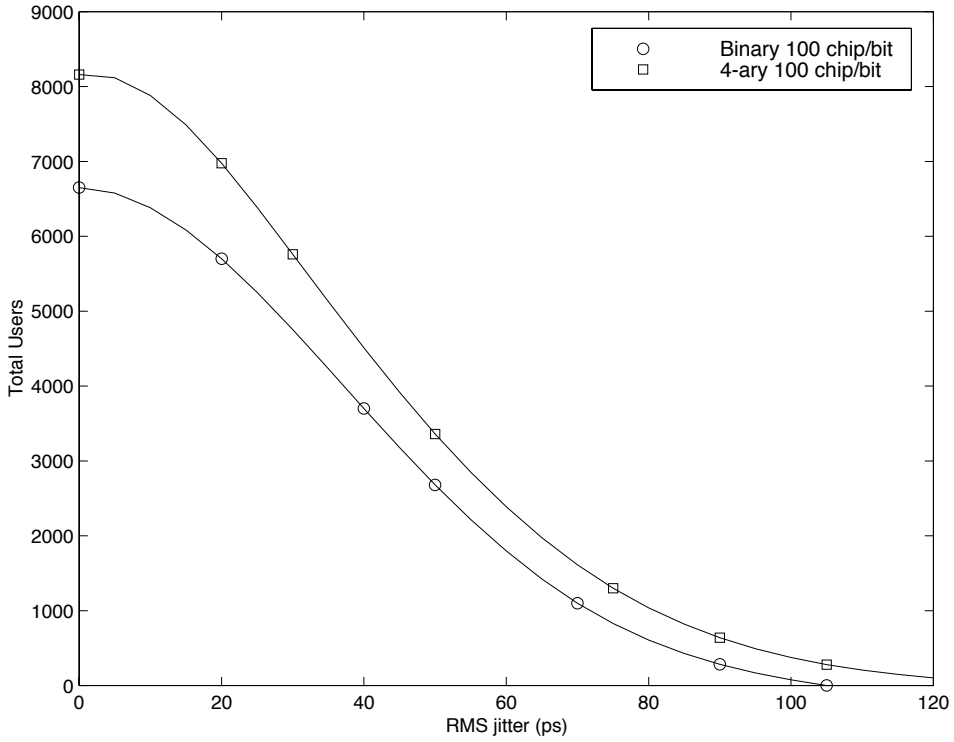

Figure 2.3: Maximum number of users supported as a function of clock jitter for binary antipodal and 4-ary orthogonal signaling.

by taking advantage of M-ary PPM signaling as described in [6]. A 4-ary orthogonal PPM signaling was used with the same timing jitter and interference limited channel and then compared in Fig. 2.3. From the figure we see the advantage of 4-ary signaling for the 100 chip/bit case. Note that 4-ary signaling degrades to the peak binary throughput level with as little as 22 ps RMS jitter. In an interference limited channel higher order M-ary signaling can be exploited in trade against a link timing error budget. Never the less it's apparent that degradation in performance of M-ary PPM is very sensitive to small increases in timing jitter and is thus an issue for high throughput systems.

Jitter In AWGN

In this section the effects of timing error where thermal noise dominates the interference is considered. This would be especially true of lower bandwidth tactical covert links operating close to the noise floor. Again using the same models and a 10^{-3} BER figure of

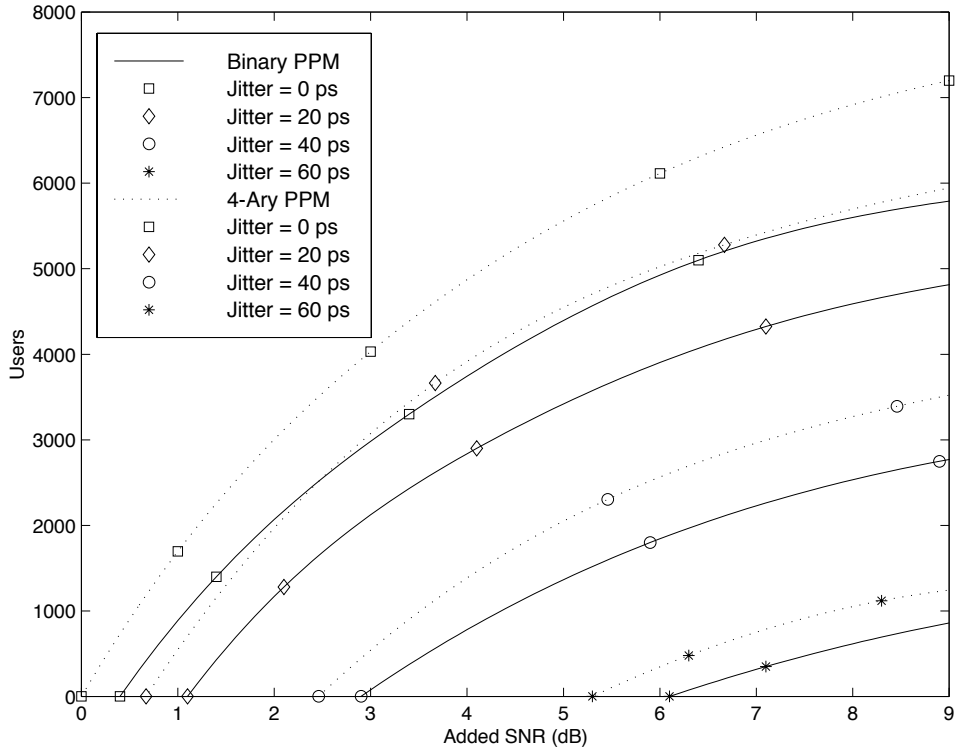

Figure 2.4: Supported users in thermal noise for 3 values of jitter, binary antipodal and 4-ary orthogonal.

merit, the number of supported users is shown in Fig. 2.4 for several values of timing jitter.

The SNR is referenced to the zero jitter 4-ary PPM performance in AWGN only. The advantage 4-ary PPM has here in AWGN is due to the slight loss associated with the offset binary PPM matched filter over an ideal antipodal matched case. Because of this and our defined minimum operating performance, the 4-ary PPM system out performs binary offset PPM at all jitter levels in thermal and pulse noise. For our consideration here of more covert, low power, and low data rate links, the advantages are more modest than those seen at higher pulse densities. The benefit of 4-ary PPM relative to the offset binary case is even more diminished with increased timing jitter at these same levels. Considering the additional complexity required for M-ary PPM decoding and tracking, this added complexity in lower throughput applications may not be worth the expenditure if clock jitter is much above 40ps.

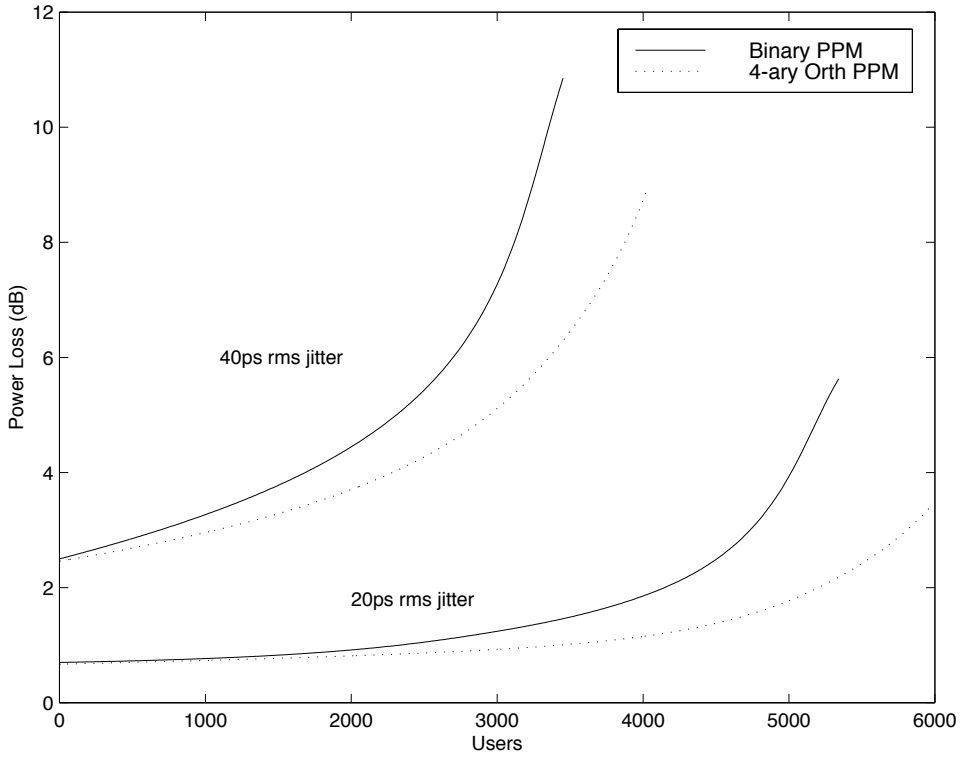

Figure 2.5: Added power required to maintain throughput as a function of the number of users.

The additional power required to compensate the timing degradation at these lower throughputs is far less than the additional power required at higher throughputs. Consider the added power required to compensate a 1000 user system for 40 ps of timing error (3.2 dB above reference) verses a 3000 user link requiring an additional 4 dB to 7.2 dB above reference. This relationship between system throughput and timing jitter is illustrated in Fig. 2.5. For relatively low throughput, low power systems, the power penalty for jitter is far less. For example, it may be beneficial for covert, low capacity sensor systems to trade jitter performance for related clock power field support life. Alternatively, as the throughput of the system increases, the added power required to compensate for timing degradation becomes quite large. This is due primarily to the environment becoming more pulse interference limited approaching the asymptotic limit on maximum throughput for a given timing error.

For extreme jitter cases the offset binary method will tend to fall off faster than the

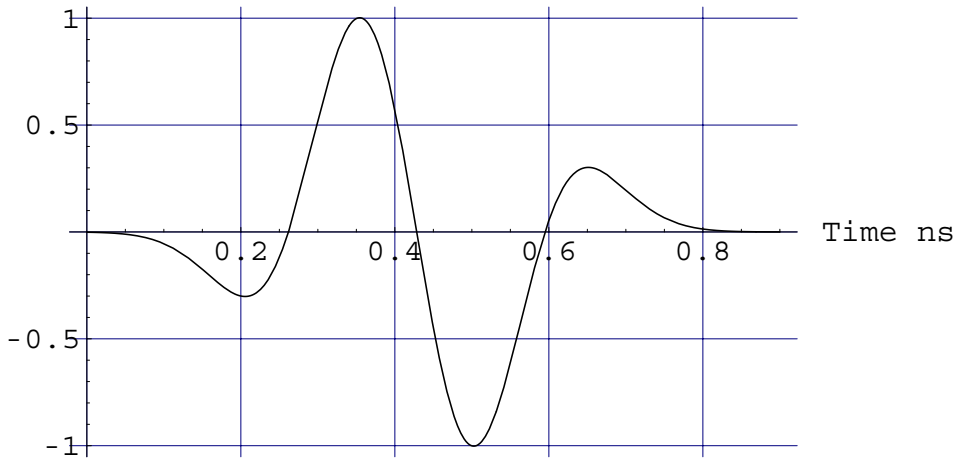

Figure 2.6: Normalized correlator template for the binary antipodal case.

orthogonal method. For this case it's easy to see that the probability of erroneously sampling near the steep transition of the impulse response in Fig. 2.6 will add large errors as compared to the orthogonal single pulse response. Note that 4-ary PPM signaling degrades more gradually than the binary case due partly to the nature of the matched filter used.

2.2 Tracking Methods

2.2.1 Early-Late Gate Tracker

A straightforward, orthogonal M-ary tracking architecture is depicted in Fig. 2.7. Normally the tracker is shown with two matched filters to the pulse (2.9), offset around the sampling instant. In this case we combine the early minus late filter error into one filter as we do for the binary position decoder for IR in (2.4). For IR the sampled error must be summed over a multiple chip interval, defined here as N_t. This summation duration may span several symbol periods depending on the design, so further accumulation may be required at the symbol rate. Detection of the symbol determines which offset error accumulator is selected for input to the filter. The filter we use is a simple implementation of an α/β tracker

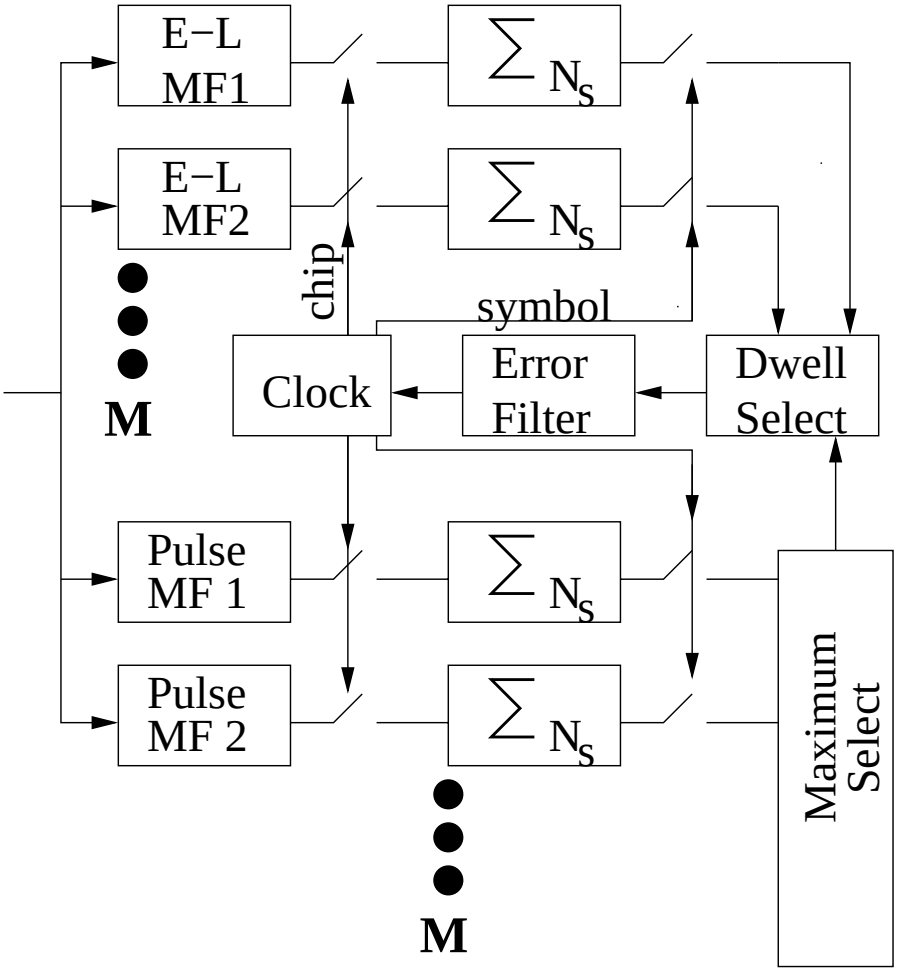

Figure 2.7: Block diagram showing the receiver signal processing. The model includes the early-late gate tracker [1] and bank of matched filters corresponding to each of the *M* waveforms in the signal set.

weighting the error history by β, i.e.,

$$\varepsilon_i = \alpha\varepsilon_m + \beta\varepsilon_{i-1}$$

where ε_i is the error out of the tracker at time i, ε_m is the "raw" sampled error, and α and β are weight factors.

The resulting error is mapped against the S-curve characteristic based on the offset selected for the early/late filter. Clock updates to chip and symbol timing for tracking and detection occur at a rate of $N_t \times T_c$.

Tracking Simulation

The early-late gate tracker [45, 1, 46] typical of narrowband systems was applied to Impulse Radio and indicated RMS jitter values around 10 ps at equivalent operating thresholds. The complexity of this tracker was kept relatively simple, with single symbol period tracking updates and $N_t = 200$ chips to illustrate the IR tolerances involved. Timing jitter added to the source and receiver did not tend to degrade the RMS jitter out of the tracker but did reduce lock stability. Never the less, with zero clock offsets, nominal timing jitter and allowing enough loop bandwidth to track small drift rates the tracker will contribute timing errors to the overall budget. Even with very good design under nominal offset conditions it's not hard to see a timing jitter link budget error become a significant consideration.

The narrow pulse nature of IR makes for a rather short position error discrimination "S" curve as illustrated in Fig. 2.8 The family of curves represent early and late offsets from 70 ps to 150 ps. These curves show the difference between the early and late filter normalized by the peak pulse detection level to account for dynamic range effects. The results observed here were obtained with an early late offset of 150ps and error damping coefficients $\alpha = 0.1$ and $\beta = 0.9$. This narrow discrimination curve characteristic makes for instability and requires added complexity for detection of rapid drift rates and fast reacquisition. Long integration periods limit tracking rates but improve nominal stability. To obtain the anticipated performance of IR, all of these performance issues must be mitigated

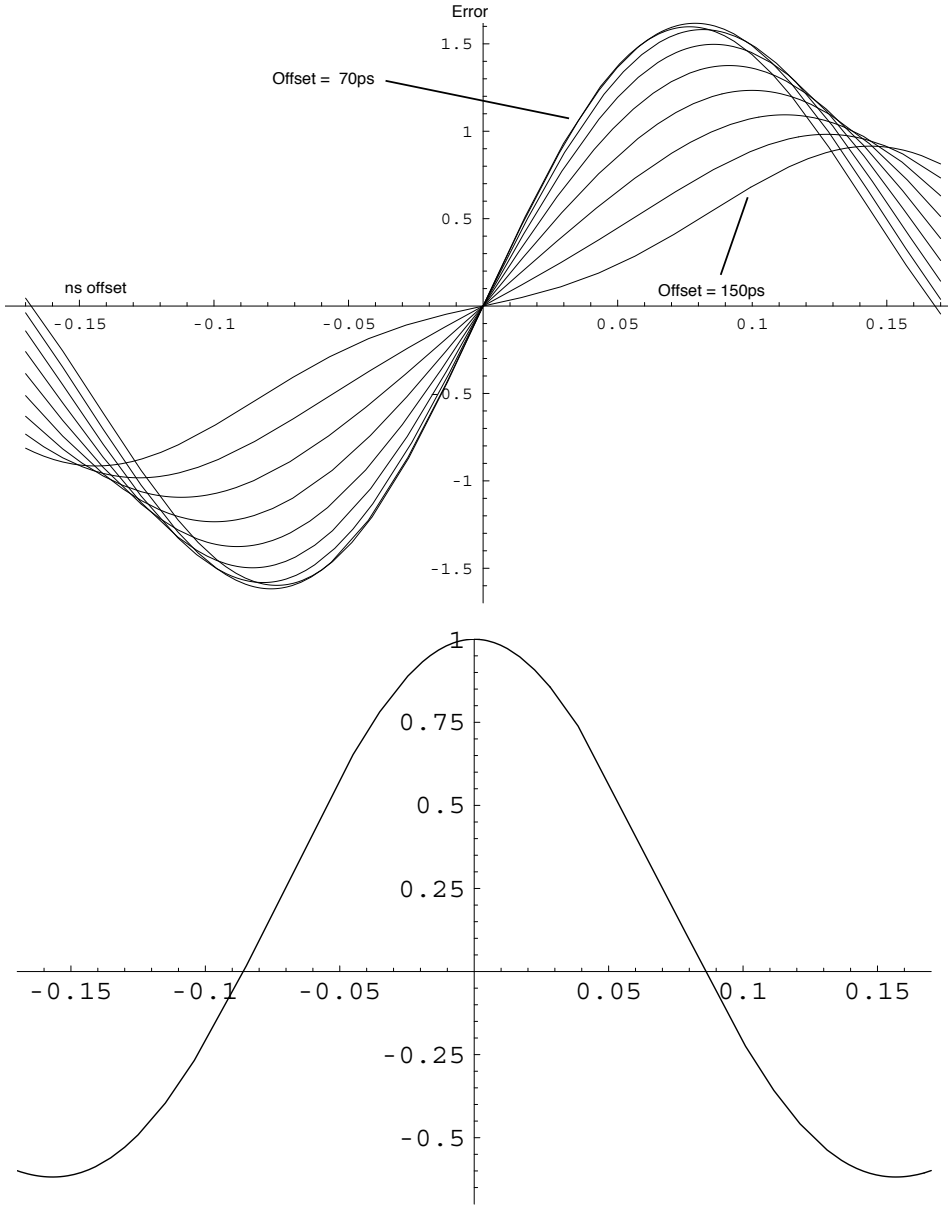

Figure 2.8: Position error “S” curves for early and late offsets from 70 ps to 150 ps with the normalized pulse autocorrelation response for the same interval.

with additional complexity. Orthogonal M-ary signaling requires parallel position error integration prior to symbol detection. Selection of the resulting position error is directed by the detected symbol. Data assisted tracking with symbol errors for the orthogonal case will simply incorporate noise into the tracking filter.

A tracker for binary offset signaling configured the same way must deal with the relatively close positions with $\delta = 156$ ps in $v_{bit}(T)$. Bit error decisions in this case will include bias errors into the tracking filter rather than just noise making operation below 10^{-3} BER very unstable. Thus, timing tolerances imposed by IR add complexity beyond the simple application of common narrowband tracking techniques.

2.2.2 Error-Tracking Synchronization Method

Applying traditional narrowband tracking techniques such as an Early-Late gate tracker, as described in section 2.2.1, can be rather complex and awkward for a time domain method like UWB. A much simpler and efficient tracking method can be borrowed [2, 47] from maximum likelihood baseband Pulse Amplitude Modulation (PAM) methods . Also related in the literature [45] to error tracking synchronizers.

Consider the maximum likelihood method for estimating the timing offset τ with the log-likelihood function given by

$$\Lambda_L(\tau) = C_L \sum_k a_k \int_{T_0} x(t) g(t - kT - \tau) \tag{2.13}$$

$$q_k(\tau) = \int_{T_0} x(t) g(t - kT - \tau) dt \tag{2.14}$$

where $g(-t)$ is the matched filter to the pulse and a_k, in this case, the binary symbols. The estimate is obtained [2, 47] from differentiating the log-likelihood function.

$$\frac{d\Lambda_L(\tau)}{d\tau} = \sum_k a_k \frac{d}{d\tau}[q_k(\tau)] = 0 \tag{2.15}$$

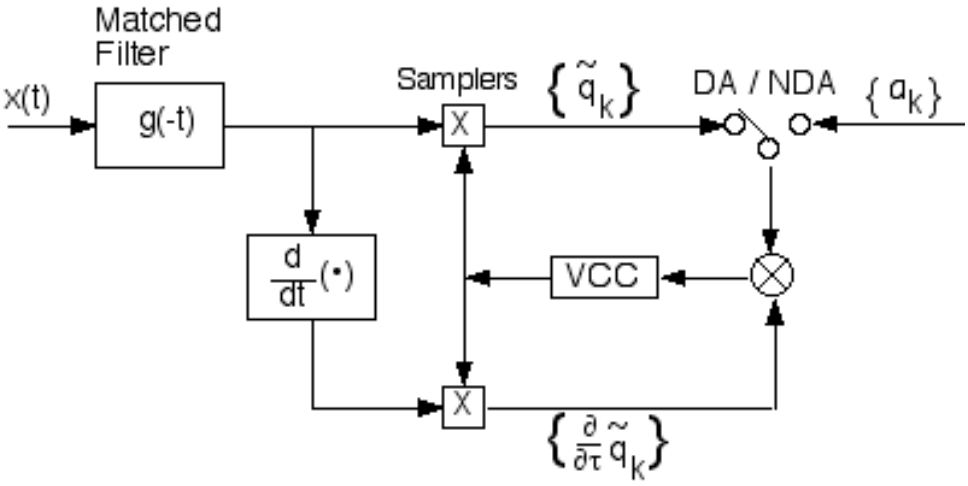

Figure 2.9: ML PAM timing recovery circuit [2]

The optimum timing is obtained when the derived timing $\hat{\tau}$ forces the equality in (2.15). An example of such an implementation is illustrated in Fig. 2.9 where a_k is selected for a decision directed estimator. The Voltage Controlled Clock (VCC) is used to advance or retard the sample time to maintain the equality required in 2.15. Note as well in Fig. 2.9 that we can use the received symbol $\tilde{q_k}$ as part of a non-decision directed technique.

It is possible to build such a simple detector and tracker for the classic binary PPM modulation for UWB. Fig. 2.10 shows the basic architecture used for simulation. It implements a single matched filter for decoding and another for tracking. This filter impulse response $h(-t)$ is just the PPM response used for binary offset modulation. The tracking filter is the equivalent matched derivative as illustrated in Fig. 2.9. The MF output and tracking filter are sampled at the chip rate and then summed over a bit period. It should be noted here that the thresholding for bit discrimination described later in Chapter 3 can be implemented in not only the symbol detection path but as part of the tracker as well. Timing from the VCC is used for chip sampling as well as symbol sample timing. This illustration uses $\tilde{a_k}$ as a non-decision directed tracker but this can be easily modified for decision direction as part of known packet preambles or simply a separate timing channel.

A tracking loop filter $F(z)$ is added for improved stability and noise reduction. Generally lower order loops are considered such as that used in [48] for analytical analysis of

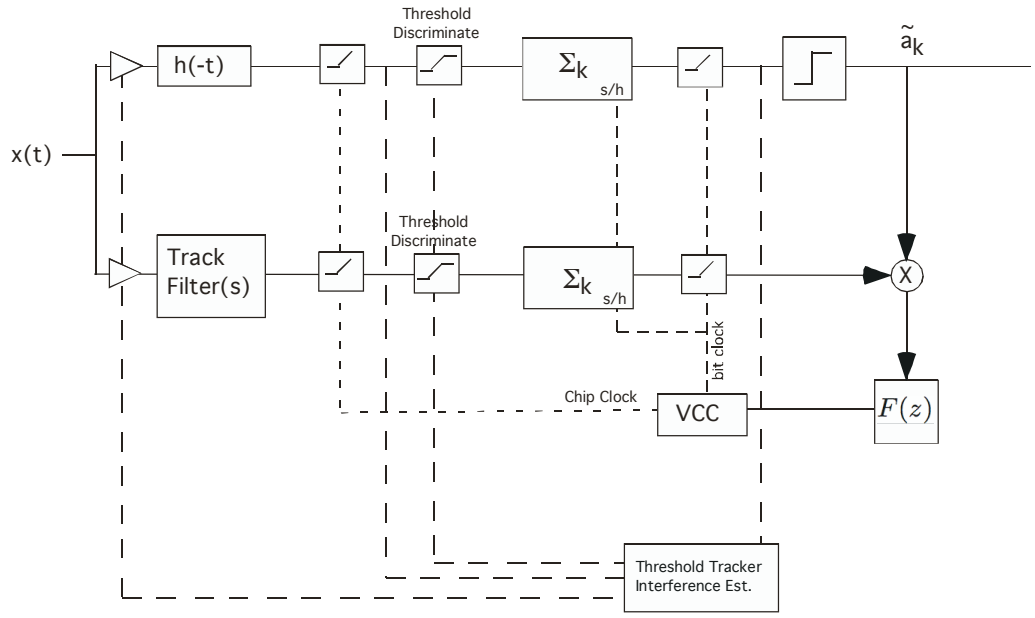

Figure 2.10: Error Tracker Block Diagram

loop stability. Similarly we use a first order low pass filter

$$F(z) = \frac{z\,(1-\tau_a)}{(z-\tau_a)} \tag{2.16}$$

where τ_a is set for bandwidth and response characteristics. Although the input signal has zero mean, and thus does not contain the traditional narrowband deterministic periodic component exploited by a Phase Locked Loop (PLL), there is still some periodicity embedded in the input signal because of it's cyclostationarity with the frame period [45]. For this type or error tracking recovery we will assume a linear offset error gain so we can derive the closed loop performance $H(z)$.

$$H(z) = \frac{K_d\,K_0\,z\,(\tau_a-1)}{z^2+\tau_a-z\,(1+K_d\,K_0\,(\tau_a-1)+\tau_a)} \tag{2.17}$$

K_d and K_0 form the loop gain with K_d the timing error detector gain and K_o the integrator or filter gain in this case. The values of τ_a and the loop gain selected for the binary offset

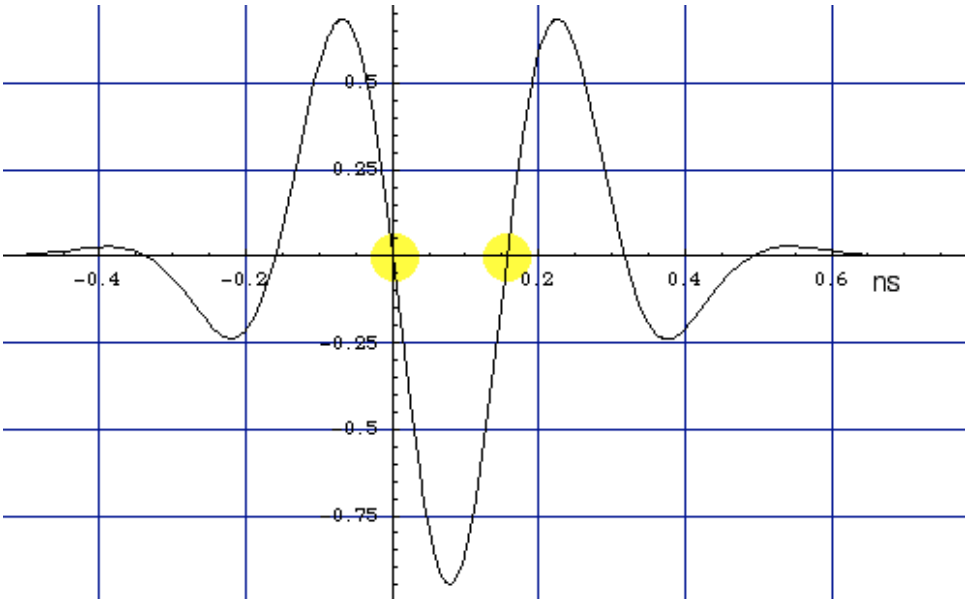

Figure 2.11: Error discriminator response for binary offset modulation method.

response used was selected to keep the bandwidth narrow for noise immunity but wide enough for realistic clock drift rates. The low order loop also ensures stability as seem in Fig. 2.12.

The timing error discriminator response is shown in Fig. 2.11. The two highlighted zero crossing points are the binary offset timing positions. The slope of the position error out of the timing error path will depend on the data modulated PPM position. Because of the symmetry of the response the slope can be corrected using either the decoded bit ± 1 polarity or a known binary data assisted preamble. The data corrected sample timing errors can now be averaged over m bit periods to correct the VCC. In this implementation no squaring or other nonlinear function is used to average over unknown symbols.

The deviation from a linear discriminator based on the slope at the origin is illustrated in Fig. 2.13. The timing offset error associated with correcting for the wrong symbol (”0” or ”1”) is more significant for greater offset values. Borrowing from linear sinusoidal tracking theory [45] an expression for the variance of the timing estimate $\tilde{\tau}$ given by,

$$var[\tilde{\tau}] = \frac{T}{K_D^2} \int_{\frac{-\pi}{T}}^{\frac{+\pi}{T}} [H(e^{j\omega T})]^2 S_N(e^{j\omega T}) \frac{d\omega}{2\pi} \tag{2.18}$$

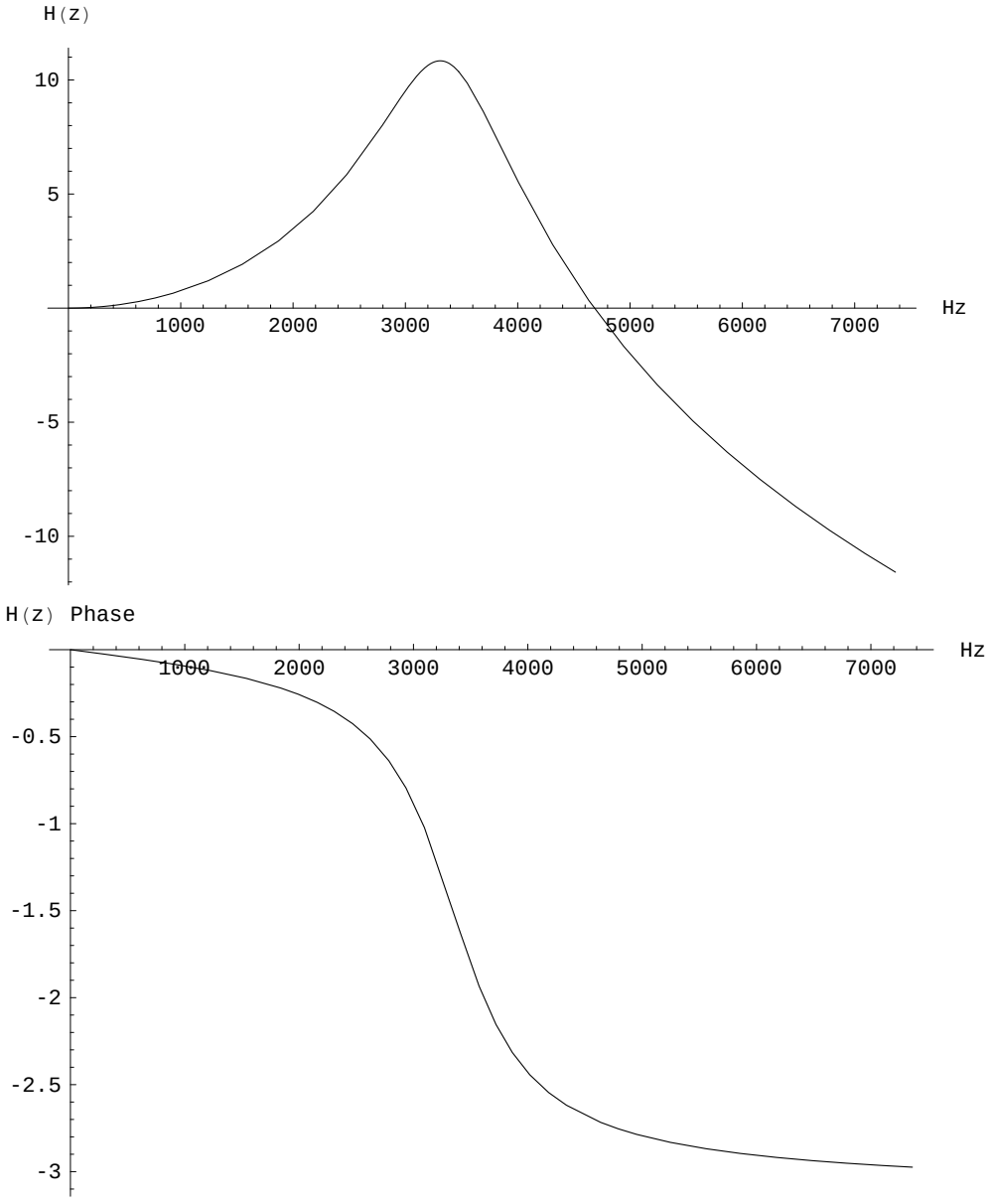

Figure 2.12: Tracking loop gain and phase characteristics

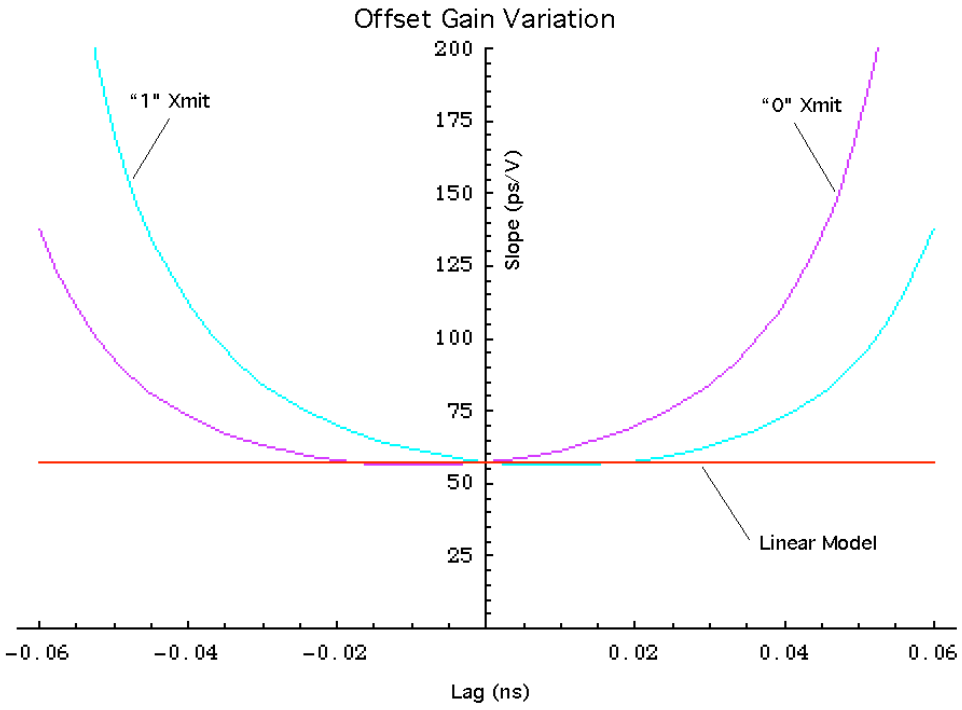

Figure 2.13: Slope error associated with offset and data polarity

with the loop noise distribution S_N, shows how sensitive the this estimate will be to the variation in the discriminator gain coefficient K_D. It is clear from both figures that timing error offsets for tracking must be maintained within a very narrow window to maintain reliable updates to the loop filter as well as reasonably predict tracking performance with linear models. This tolerance is consistent with the timing errors described for data detection in Chapter 2.

Simulation

With the concern for timing tolerance and it's potential effect on link performance described in section 2.1 we constructed a simulation based on Fig. 2.10 to derive some estimates of what effects tracking errors might impose. The same link parameters used in section 2.1 are used again here. The chip rate is set at 100 chips/bit with the chip frame rate $T_f = 128$ ns. The coefficient used for the loop filter is $\tau_a = 0.9875$ and consistent with the characteristics of Fig. 2.12.

In addition to the jitter and timing bias errors that we have analyzed previously, the tracking loop lock performance is also of great concern. This is especially important since timing acquisition can be a potentially time consuming process for IR. Typically this performance is measured as the mean time between lost lock (MTLL) [49], or cycle slips in the literature of PLL implementations. Typically analytical results in closed form for sinusoidal Phase Locked Loops (PLL) are only obtainable for 1^{st} order loops [45]. Even for higher order sinusoidal tracking loops, very sophisticated series expansion based numerical methods are needed. Impulse Radio characteristics would certainly add complexity to this analysis. A first order loop expression for expected cycle slip time in a PLL can be approximated as [45]

$$2\, B_L\, E[T_{slip}] \cong \frac{\pi}{2}\, e^{2\rho'} \tag{2.19}$$

where ρ' is the loop SNR and B_L the one sided loop noise bandwidth. It is reassuring to note that simulation results for IR show similar MTLL exponential relationships with respect to SNR and loop bandwidth.

A simulation of the error tracker in Fig. 2.10 for Impulse Radio was run in a non-data assist mode with assumed random known data correcting the slope error. The MTLL for this case is shown in Fig. 2.14. Due to the extensive simulation time required SNRs were limited to MTLL rates below 20 to 40 minutes. The log linear nature of this performance curve allows reasonable extrapolation to longer MTLL periods. The combination of a high chip per bit rate and a narrow loop filter allow for reasonable MTLL periods at lower SNRs. The addition of an equal power user density to the thermal noise will degrade the SNR and also changes the slope of the curve. As we have noted before the occasional collisions from local interferes can be more destructive than thermal noise effects.

If however we assume data assisted tracking using decoded symbols to correct the tracking offset error, the performance is limited by the BER performance. The noise induced by these errors significantly degrades MTLL performance as compared to the previous results shown again in Fig. 2.15. Our assumed metric BER rate near 10^{-3} for a data link does not degrade tracking performance significantly. The 6 dB difference between data assisted and non-data assisted tracking suggests a possible implementation of a separate timing channel from that of the data link. Since acquisition is assumed a latency issue it

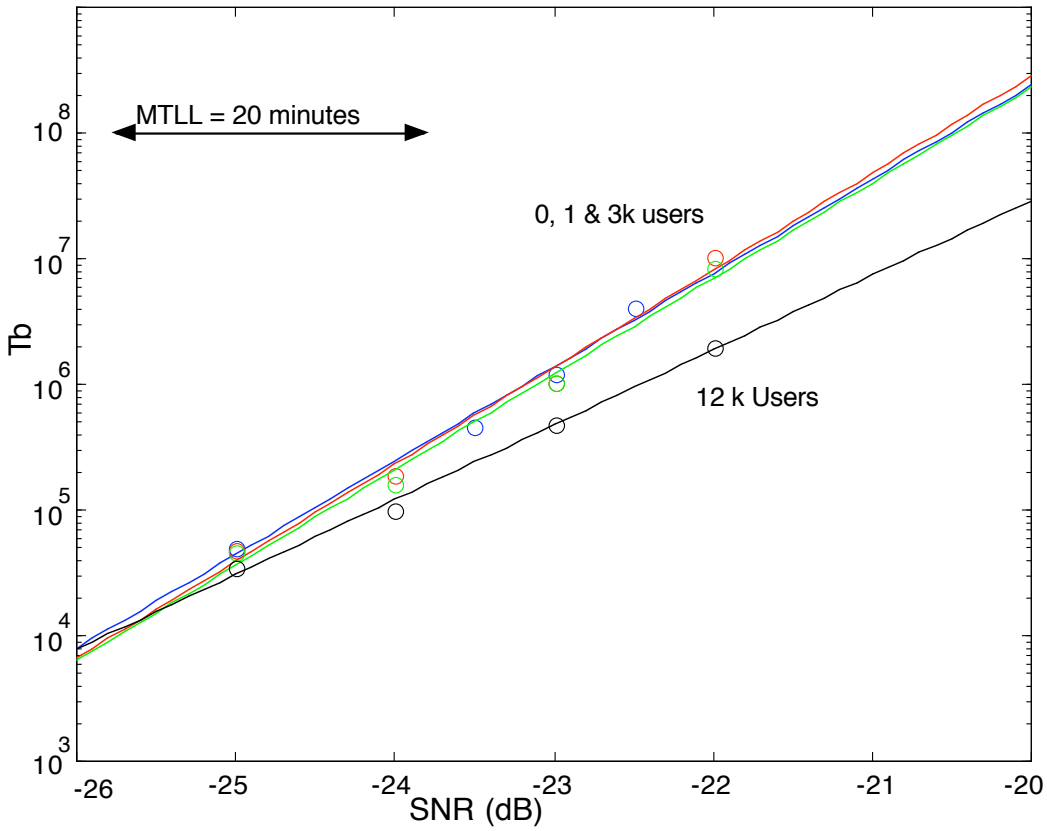

Figure 2.14: Equal power multi-user density effects on MTLL

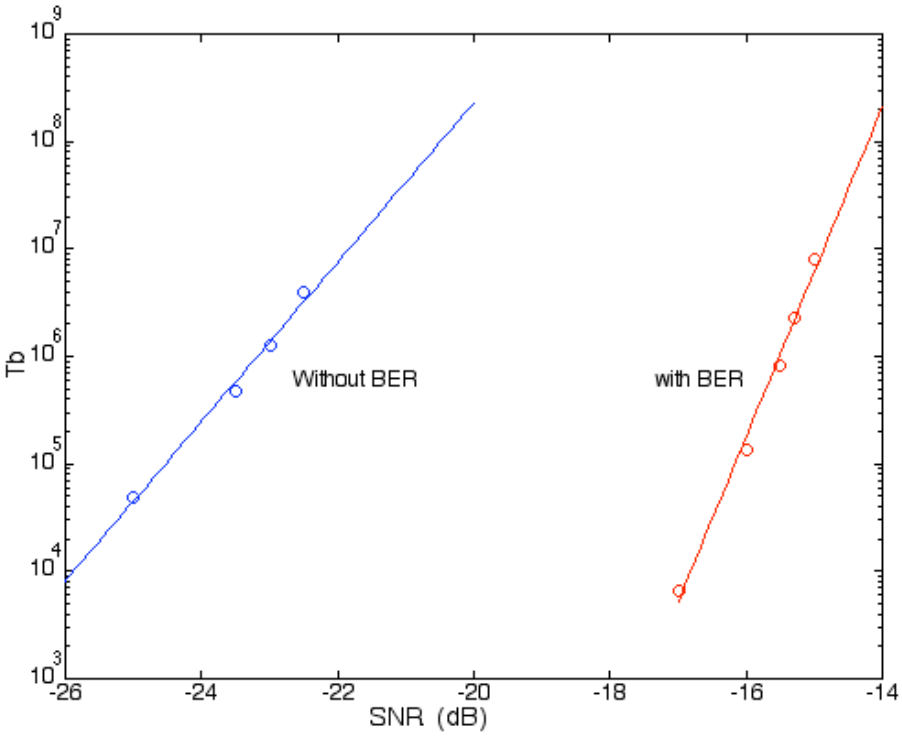

Figure 2.15: MTLL with effects of bit errors in the tracking loop.

may be better to maintain a lower power tracking channel as a timing source for a packet burst of data at a higher power. This would have the desired effect of reducing latency for rapid data packet transmission with a potentially low observable tracking network. The data packet link could even be on a separate hopping code and still derive accurate timing from the tracking link. This would have the advantage of not exposing the tracking link to observation at higher powers and thus maintaining a degree of covertness.

We have noted the deleterious effects of timing jitter on IR performance but timing derived from a tracking loop can also add bias offsets when tracking drifting or offset clocks. Under static conditions it would not be unreasonable to expect the correction of clock offset biases with little additional complexity to the tracking logic. When transponders are in motion however, the resulting clock drift or ”pull” may not be adequately tracked and corrected. Under these conditions, noting the non-linear timing discrimination curve in Fig. 2.11, a bias offset could not only under correct a linear model but place the operating point

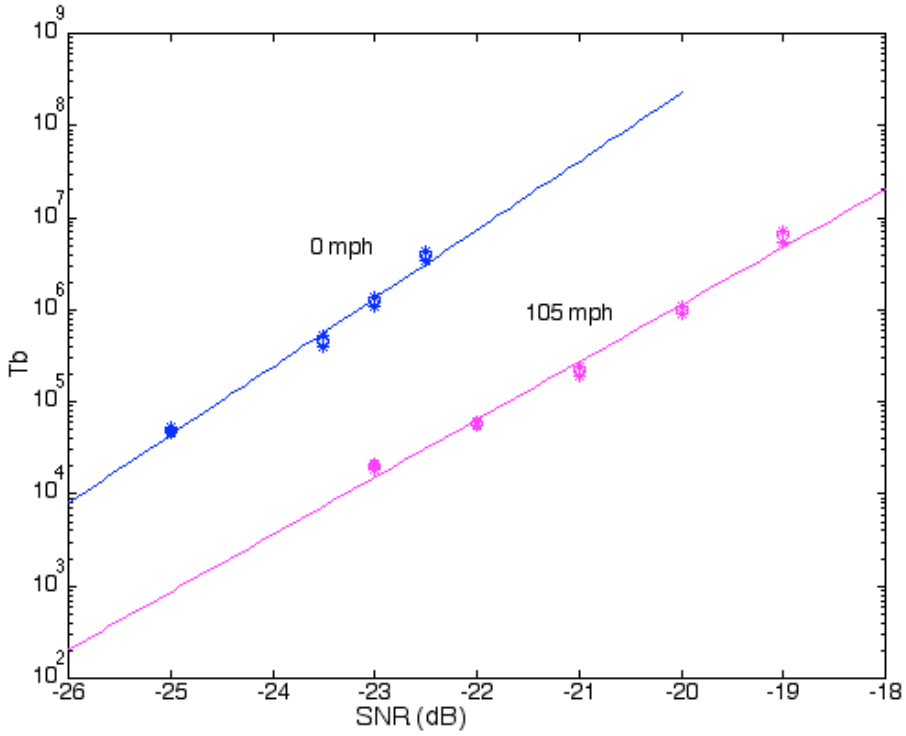

Figure 2.16: MTLL with effects of clock pull at an equivalent velocity of 100 mph.

closer to the end of the monotonic tracking region. The effective tracking region, for the same noise variance, will be reduced and increase the potential for the loss of lock. To illustrate this we consider a transponder traveling at a velocity varying from +105 mph to -105 mph relative to a static source. This velocity is equivalent to a clock offset of 2 ps per bit period. The MTLL performance for non-data assisted tracking with velocity offsets is compared in Fig. 2.16. For the simple first order tracking loop considered here, the effects are significant at the lower SNRs. IR operating under such conditions would likely implement separate tracking logic to compensate for these relatively slow clock drifts. Temperature and tolerance induced drifting between clocks are reasonably deterministic and correctable with very narrow tracking loops.

Just as we described the multi-user performance degradation associated with clock jitter in section 2.1 the same clock jitter can influence tracking performance. The non-data assisted tracking loop was considered with end-to-end clock jitter levels of 20 ps and 40 ps.

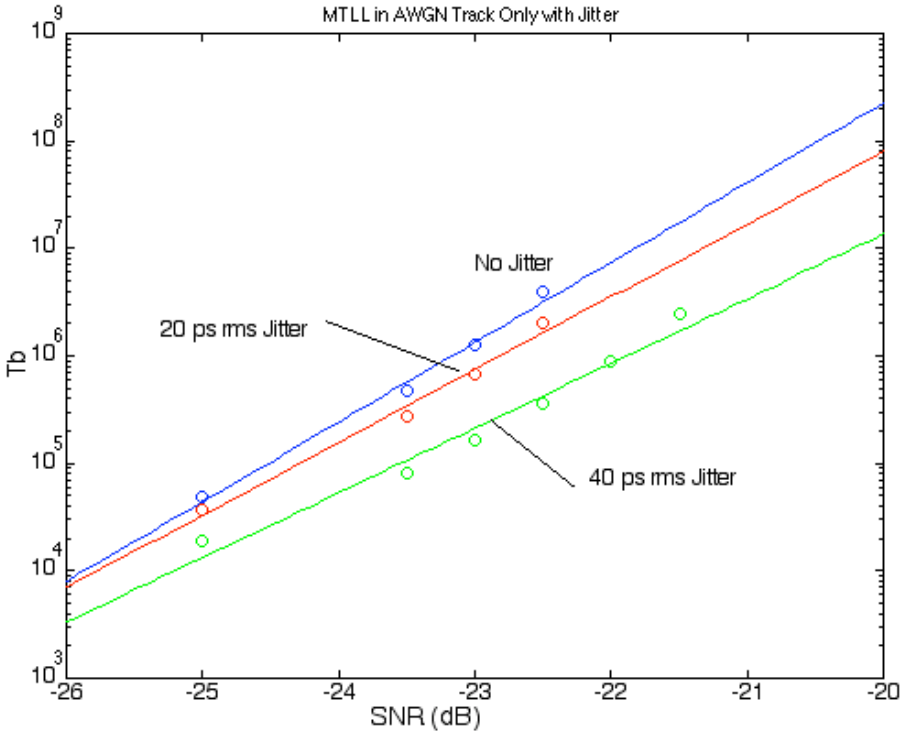

Figure 2.17: MTLL with effects of clock jitter.

The MTLL performance for jitter is illustrated in Fig. 2.17. It's obvious that the added jitter or variance at the discriminator is not as deleterious to MTLL performance as bias errors associated with clock offsets illustrated in Fig. 2.16. The 40ps jitter performance was 2 dB worse than that of a perfect clock. Not only does clock jitter degrade the data link performance , as described in section 2.1, but may even further degrade this performance by compounding additional error derived from the tracking loop.

Assuming we can maintain timing with reasonable MTLL we now consider the effects on link BER performance deriving sample timing from the proposed tracker. Fig. 2.18 shows BER performance for various tracking conditions without assumed clock jitter. The SNR is limited by BER performance for the 100 chip per bit gain selected. The non-data assisted tracker at this SNR adds little performance degradation. The effects of data assisted tracking can be seen at the lower SNRs but converges to near ideal timing at BER rates of interest. Operating the tracker at these higher SNRs not only maintains a very high

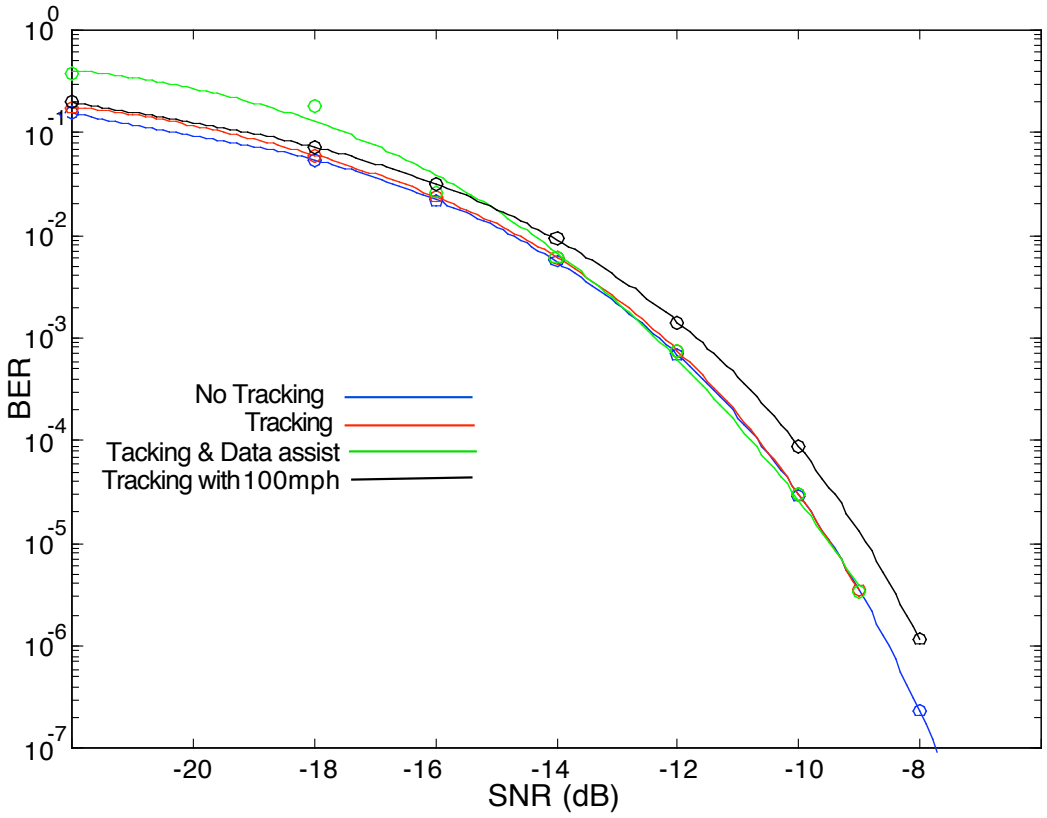

Figure 2.18: BER performance with Tracking without timing jitter sources

MTLL but provides nearly ideal sample timing for data decoding. Even the addition of an equivalent 105 mph clock offset only degrades BER performance by a fraction of a dB. The MTLL performance of the tracker with this clock offset will also still be quite long.

Consider now the sample timing derived from the tracker with clock jitter added to the transponder shown in Fig. 2.19. The addition of 40 ps of jitter to the tracking channel degrades performance by 2 dB at a 10^{-3} BER. Most of this appears to be attributable to jitter alone. The tracking filter seems to handle this jitter well at this high SNR adding little additional loss to timing induced errors. If we now consider a data assisted tracking loop with jitter and clock pull the performance falls off 5 dB from ideal timing. Most of this additional loss would be associated with the clock offset since the BER at this point is small.

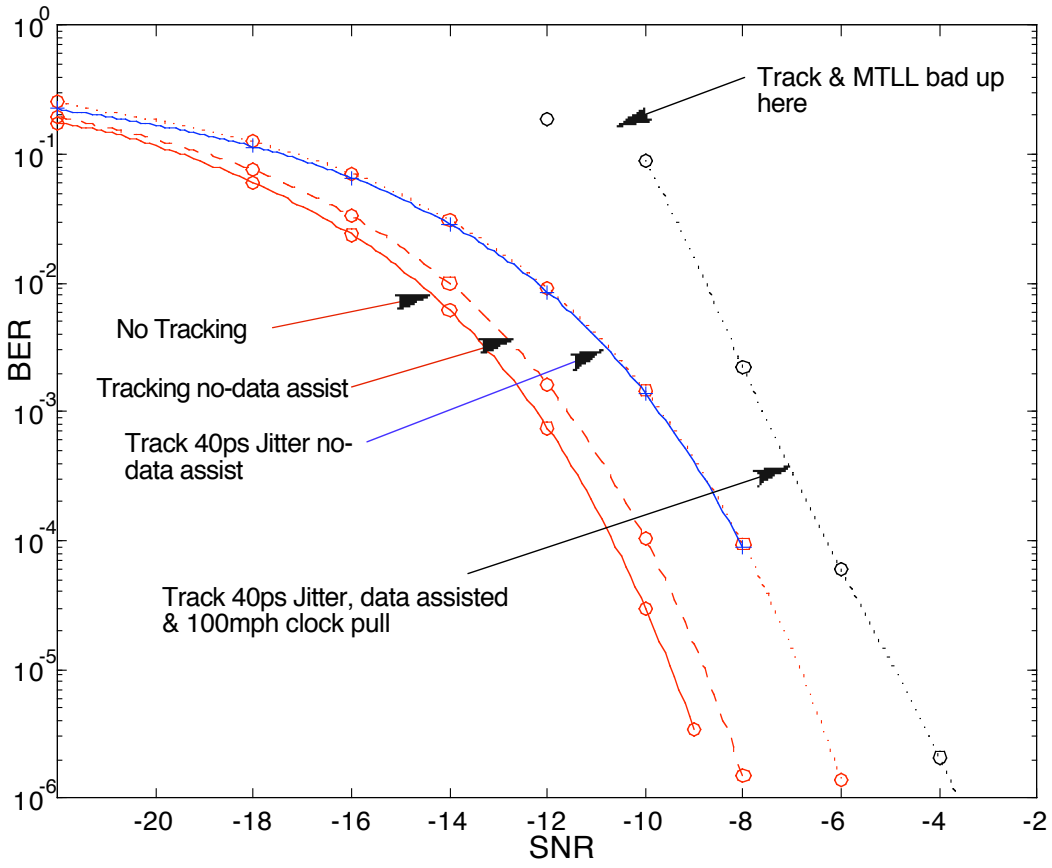

Figure 2.19: BER performance with Tracking with timing jitter sources

2.3 Conclusions

The narrow pulses used in impulse radio place stringent requirements on timing. This chapter investigated the effects of timing jitter and tracking on the performance of binary and orthogonal 4-ary impulse radio systems over a range of pulse interference levels. For a fixed bit error rate, the relationships between the number of multi-access users and RMS jitter levels were quantified. The results show that system throughput degrades markedly for relatively modest increases in jitter. For the parameters used in our studies, we find that 4-ary PPM out performs offset binary PPM for all timing errors but that this advantage diminishes with increased jitter.

In light of this extreme sensitivity to timing errors we consider the effects of tracking on Impulse Radio and what methods may be applied. To highlight some of the issues associated with IR we first consider what it would take to implement a traditional narrowband tracker. An early-late gate tracker is implemented to show one of the familiar contributors to overall link budget jitter. Results of the simulation show tracking jitter contributions of 10 ps RMS for thermal noise and pulse densities consistent with 10^{-3} BER environments. This method is however rather clumsy when dealing with a time domain modulation like Impulse Radio.

A more appropriate method based on error tracking techniques was developed for IR. This technique is much less cumbersome that the early-late gate tracker and illustrated the performance advantages of a narrow band closed loop feedback filter. In addition to the jitter considerations, simulations were used to show anticipated mean times to lost lock. A very important consideration given the potentially long acquisition times required for IR. Model performance illustrating the effects of user density, clock offsets, data assist errors and jitter are presented for loss of loop lock as well as a source for decoding performance. The timing tracking loop performs well under nominal ideal clock characteristics adding little decoding loss at high SNRs. Adding the practical influences of source jitter and clock offsets can significantly degrade tracking assisted decoding.

Chapter 3

Autonomous Near - Far Power Adaptation with Chip Discrimination

Impulse radio (IR) employs sub-nanosecond pulses to support high throughput multi-user densities. The very nature of these low duty cycle narrow pulses limits the potential for pulse-on-pulse interference in uncoordinated environments. Theoretical capacities of UWB systems [4, 7, 50] are typically derived assuming identical receive powers for all users. However pulse collisions where near far power ratios are large can greatly limit performance and capacity for UWB. If co-located transponder hopping codes are not orthogonal or synchronized for blanking the resulting noise power added to the bit decision sum can significantly reduce BER performance. Typically systems have used coordinated power control or synchronized blanking [27] to maintain link quality BER constraints. Acquiring timing of near users for purposes of receiver blanking adds complexity and potential latency to a system. It also may not always be possible to acquire near neighbor timing. Coordinated power control [51] also adds a layer of complexity to the overall system and requires user compliance. In high density buildings, for example, commercial systems would potentially have to adapt to many types of UWB links operating within feet of each other requiring standards for cooperation. Tactical systems, to an even greater degree, will

likely have to contend with uncoordinated hostile systems and jamming.

This chapter proposes a very simple passive technique to address these issues of power disparity between users. Typically a bit (or symbol) is spread over a number of chips N_s where hopping sequences between users are assumed to be independent and pseudorandom. A typical receiver for IR uses a matched filter sampled at the hopping interval for the selected user. The accumulated level at the sample instant of the matched filter is summed with all N_s samples for each bit or symbol. The resulting sum is then used for symbol decisions.

Assuming a relatively large near-to-far power ratio this proposed technique applies an acceptance level threshold to each chip sample prior to summing for symbol decisions. Without this discrimination a chance hit in the narrow chip correlation window by a very strong pulse can erroneously bias the symbol decision. By discarding large level chips from the N_s sum much of the performance can be recovered, just as in the case of coordinated blanking [27], by using the surviving chips. All that is required is a threshold comparison at the matched filter output, prior to the symbol chip summer, and noise floor tracking threshold logic. The low duty cycle nature of UWB uniquely allows implementation of this selective discrimination technique not available in traditional narrowband systems.

This chapter begins with the development of an analytic model of the proposed system describing the performance dependence on threshold and interference power for a conventional binary IR system. Simulation results are compared to the analysis and used to illustrate the performance enhancements when compromised by varying near/far power ratios. Examples of multi-user densities for offset binary and 4-ary modulation are compared and optimized for chips per symbol. A comparison is then made between chip discrimination and a hard limited receiver.

3.1 System Model

For the development of this analysis the environment is assumed to have a far greater density of similar distant users representing the pulse limited background noise and the desired link level. In this near-far scenario the number of collocated transponders is nor-

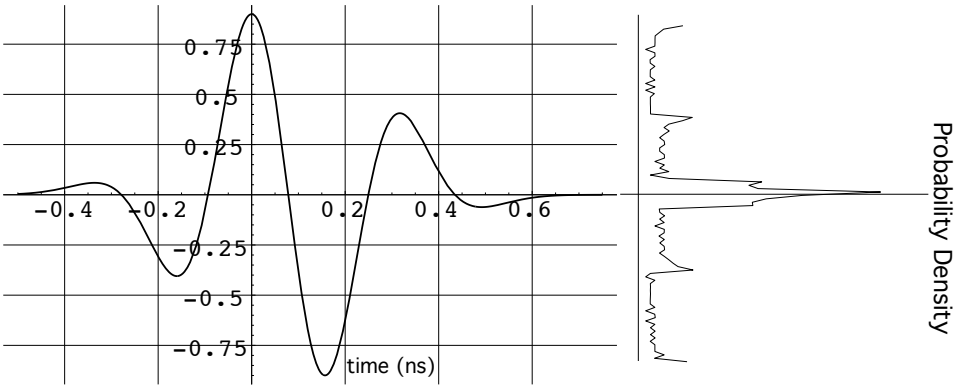

Figure 3.1: The sample level out of a matched filter for an offset PPM pulse is dependent on it's relative time of arrival. Interfering pulses with a uniform arrival time distribution demonstrate an amplitude probability distribution clustered around zero.

mally small relative to the overall population and assumed less than 10 in number. All of the interfering transponders have the same frame and pulse rates but with independent timing randomly distributed relative to the desired link. The resulting noise from a chip matched filter for a large number of distant interferers is assumed to be a Gaussian source with variance given by

$$\sigma^2 = N_{bg} \frac{\tau_{mf}}{T_f} {\sigma_{mf}}^2 \tag{3.1}$$

With N_{bg} pulses per frame time T_f, the noise variance of the equal power transponders σ^2 is the average number of expected pulses randomly distributed in the filter window τ_{mf} times the variance out of the chip filter for uniformly random correlation times ${\sigma_{mf}}^2$. The matched filter used here is a binary offset filter as described in [4, 5, 13] and shown in Fig. 3.1 with time scale coefficient $t_n = 0.29$ ns. The relatively small number of collocated interferers however is not only less likely to collide with the chip filter correlation window but likely only to add a single powerful pulse to the sum when one does collide. The resulting probability density distribution for these powerful collocated pulses will be approximated by the scaled density function of Fig. 3.1. Since this density distribution for random correlation output levels is very unique and the levels are predominantly clustered around zero we will use a Laplace distribution as an analytical approximation. The collocated interferers approximated by this distribution will have much higher levels and will be summed with the Gaussian background pulses. The resulting distribution of the sum of

these independent events is given by

$$Z = \alpha\, X + \beta\, Y \tag{3.2}$$

where the random variable X is associated with the Laplace distribution defined as

$$P[x] = \frac{a}{2}\, e^{-a|x|} \tag{3.3}$$

and scaled by α. The random variable Y represents the Gaussian background noise where β is normalized to 1. The density function for the near pulse sum and background noise as a function of relative near/far power α is given by

$$\begin{aligned} P[z] = {} & \frac{a\,\sigma\sqrt{\frac{\alpha^2}{\sigma^2}}\; e^{-\frac{(m-z)^2}{2\sigma^2}+\frac{(z\alpha-m\alpha+a\sigma^2)^2}{2\alpha^2\sigma^2}}}{2\alpha^2} - \\ & \frac{a\,\sigma\sqrt{\frac{\alpha^2}{\sigma^2}}\; e^{-\frac{(m-z)^2}{2\sigma^2}+\frac{(z\alpha-m\alpha+a\sigma^2)^2}{2\alpha^2\sigma^2}}\; \mathbf{Erfc}\left[\frac{(m\alpha-z\alpha-a\sigma^2)\sqrt{\frac{\alpha^2}{\sigma^2}}}{\sqrt{2}\;\alpha^2}\right]}{4\alpha^2} + \\ & \frac{a\,\sigma\sqrt{\frac{\alpha^2}{\sigma^2}}\; e^{-\frac{(m-z)^2}{2\sigma^2}+\frac{(m\alpha-z\alpha+a\sigma^2)^2}{2\alpha^2\sigma^2}}\; \mathbf{Erfc}\left[\frac{(m\alpha-z\alpha+a\sigma^2)\sqrt{\frac{\alpha^2}{\sigma^2}}}{\sqrt{2}\;\alpha^2}\right]}{4\alpha^2} \end{aligned} \tag{3.4}$$

where Erfc[ ] is the complementary error function.

3.1.1 Threshold Discrimination

Now consider only accepting chip filter output values for the symbol sum that fall within a defined acceptance interval $\pm\gamma$. The resulting noise distribution for the symbol sum will be modified by this nonlinear selection process. A Gaussian output distribution from a dense equal power pulse environment and then limited by a threshold γ defines the accep-

tance probability parameter Γ, defined as

$$\Gamma = \int_{-\gamma}^{\gamma} \frac{1}{\sqrt{2\pi}\sigma} \, e^{-\frac{(x-m)^2}{2\sigma^2}} dx \tag{3.5}$$

where m is the signal component of the user of interest. If chips are accepted to the decision sum that only fall within a $\pm\gamma$ threshold the distribution into the chip sum changes. The resulting truncated probability density function for distant equal power source levels is P_{far} which is written as

$$P_{far}[x] = \frac{1}{\Gamma\sqrt{2\pi}\sigma} \, e^{-\frac{(x-m)^2}{2\sigma^2}} \quad \{-\gamma \leq x \leq \gamma\} \tag{3.6}$$

and normalized by Γ. The notation *far* denotes distant low power received pulses and *near* for larger power co-site pulses. The same can be derived for the smaller number of chips that have near pulse interference collisions by using the distribution derived in (3.4) appropriately normalized between the limits $\pm\gamma$ and defined as

$$P_{near}[x] = \frac{P[x]}{\Lambda} \quad \{-\gamma \leq x \leq \gamma\} \tag{3.7}$$

where Λ is written as

$$\Lambda = \int_{-\gamma}^{\gamma} P[z] dz \tag{3.8}$$

The mean and variance for these distributions are given in (3.9) through (3.12).

$$\mathrm{m}_{far} = \int_{-\gamma}^{\gamma} \frac{x}{\Gamma\sqrt{2\pi}\sigma} \, e^{-\frac{(x-m)^2}{2\sigma^2}} \, dx \tag{3.9}$$

$$\sigma^2_{far} = \int_{-\gamma}^{\gamma} \frac{(x-\mathrm{m}_{far})^2}{\Gamma\sqrt{2\pi}\sigma} \, e^{-\frac{(x-m)^2}{2\sigma^2}} \, dx \tag{3.10}$$

$$\mathrm{m}_{near} = \int_{-\gamma}^{\gamma} x \, \frac{P[x]}{\Lambda} \, dx \tag{3.11}$$

$$\sigma^2_{near} = \int_{-\gamma}^{\gamma} (x - \mathrm{m}_{near})^2 \, \frac{P[x]}{\Lambda} \, dx \tag{3.12}$$

3.1.2 BIT Interval Sum

The background pulse density is always sufficient to assume that all chip filter outputs experience multiple collisions of the far type. For a relatively small number of co-site users only a fraction of the received chip frames will suffer strong co-site collisions. Combining these two classes of pulse collisions and the probability that each will survive chip discrimination is combined to yield

$$p_{chip} = p_{np} \times \Gamma + (1 - p_{np}) \, \Lambda \tag{3.13}$$

The probability of a given chip window τ_{mf} avoiding a powerful near pulse collision in the chip frame time T_f is given by

$$p_{np} = \left(1 - \frac{\tau_{mf}}{T_f}\right)^{N_{near}} \tag{3.14}$$

where N_{near} is the average number of strong co-site pulses in a frame. The resulting mean (S_{mean}) of the sum is the number of surviving chips of each type times the means (3.9) and (3.11). Necessarily the bias in the mean is assumed to be the desired signal with perfect timing but the required symmetric nature of the limiting process can shift the mean toward zero, and is given by

$$S_{mean} = N_s \, (p_{np} \, \Gamma \, \mathrm{m}_{far} + (1 - p_{np}) \, \Lambda \, \mathrm{m}_{near}) \tag{3.15}$$

As an approximation, it is assumed here that there are a sufficient number of surviving chips in the bit sum to use a Gaussian model for the binary outcome. The resulting means and variances are used to determine the BER. The variance will not only be determined by the modified output distribution but by the variance of the number of surviving chips as

given by

$$\sigma^2_{Nfar} = N_s\ p_{np}\ \Gamma\ (1 - p_{np}\ \Gamma) \tag{3.16}$$

$$\sigma^2_{Nnear} = N_s\ (1 - p_{np})\ p_{np}\ \Lambda^2 \tag{3.17}$$

The resulting variance of the bit decision sum is the sum of the variances for each type of chip in the sum. For the binary modulation case the bit error performance is the zero threshold decision integration of the assumed Gaussian distribution with mean S_{mean} and variance σ^2_{sum} which is written as

$$\begin{aligned}\sigma^2_{sum} = \ & p_{np}\ \Gamma\ N_s\ \sigma^2_{far} + m^2_{far}\ \sigma^2_{Nfar} + \\ & (1 - p_{np})\ \Lambda\ N_s\ \sigma^2_{near} + m^2_{near}\ \sigma^2_{Nnear}\end{aligned} \tag{3.18}$$

The bit error rate is therefore

$$BER = \int_{-\infty}^{0} \frac{1}{\sqrt{2\ \pi}\ \sigma_{sum}}\ e^{-\frac{(z - S_{mean})^2}{2\ \sigma^2_{sum}}}\ dz \tag{3.19}$$

3.1.3 Perfect Blanking

In the previous sections where the powerful interfering pulses are assumed to vary relative to the discriminating threshold there will be cases where pulse collisions will not be eliminated. It is interesting to consider separately the optimum performance where near transponder pulse-on-pulse collisions are always blanked and removed from the decision sum. Consider a chip discriminator that reliably removes a detected chip if a strong pulse arrives within τ_w ns of this chip. The probability that a chip survives is defined by

$$p = (1 - \eta)^{N_p} \tag{3.20}$$

for N_p interfering pulses per frame where $\eta = \tau_w / T_f$ is the probability of a single randomly distributed interfering pulse arriving in the chip detection window. The distribution of the

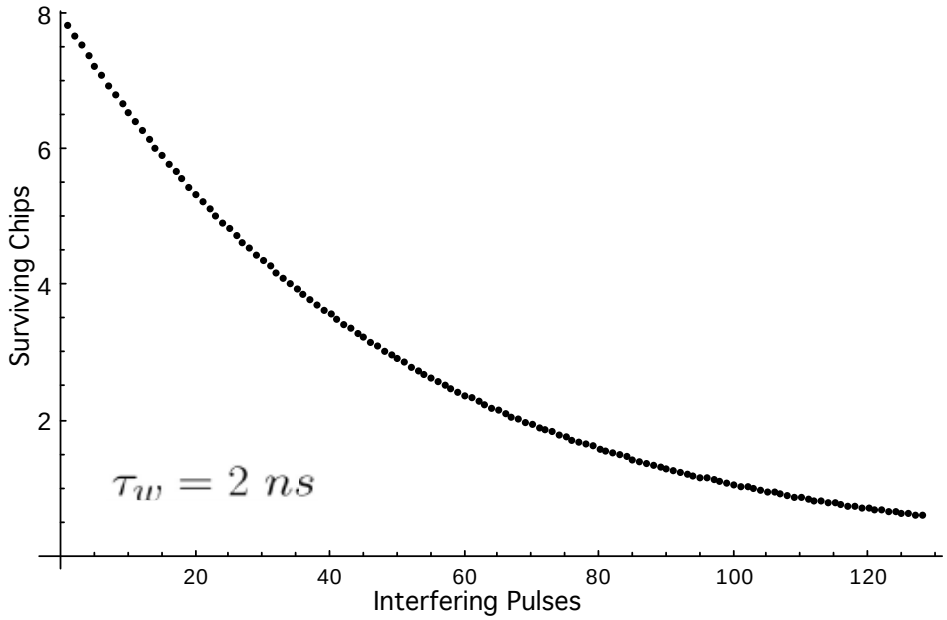

Figure 3.2: The number of surviving chips from $N_b = 8$ chips/bit for $\eta = 0.02$ and N_p interfering pulses per frame.

number of surviving chips for a frame is a binomial distribution where the expected number of surviving chips is

$$N_c = N_b(1-\eta)^{N_p} \tag{3.21}$$

for N_b chips per bit. A plot of the expected number of survivors as a function of the interfering pulse density is shown in Fig. 3.2 for $N_b = 8$ and $T_f = 100$ ns.

Assume a binary pulse position offset modulation where ε_c is the chip energy and σ_c^2 is the noise variance. The resulting bit error rate for the Gaussian noise case typical of a large pulse density is given as:

$$BER = \sum_{i=0}^{N_b} \binom{N_b}{i} (1-\gamma)^{N_p i}(1-(1-\gamma)^{N_p})^{N_b-i}\ \frac{1}{2}\ \mathrm{Erfc}\left[\sqrt{i\frac{\varepsilon_c}{2\sigma_c^2}}\ \right] \tag{3.22}$$

By scaling the chip/bit and peak power by a factor $1/N_b$ where the average power is held constant the performance for a given interfering pulse density N_p with blanking does not improve with chip spreading. Never the less the benefit of chip discrimination does require

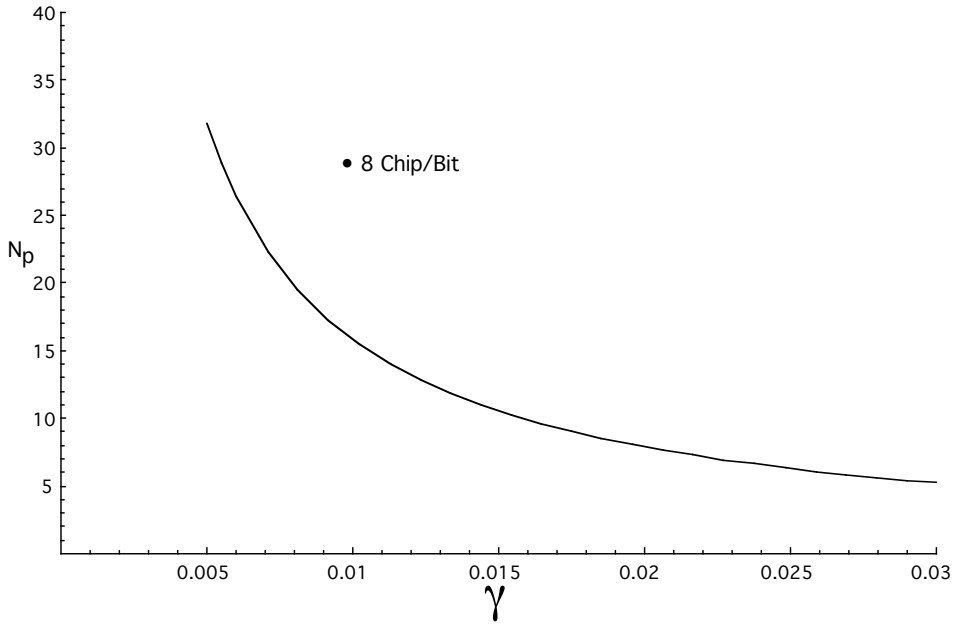

Figure 3.3: The number of sustained blanking pulses for a constant power 8 chip/bit binary offset IR link.

multiple chips per bit and the advantage of narrow pulses in discrimination is evident in Fig. 3.3. However a transponder that is only peak pulse power limited can sacrifice average power to enable better performance under adverse pulse blanking conditions. The BER performance for this case shows the advantage of raising average power by increasing only the chip/bit rate. Under the constraint of fixed peak power and perfect blanking the relationship of added chips/bit or pulse width from (3.22) and can be compared to simulation. These comparisons with IR pulses are used to derive the effective pulse-on-pulse window width τ_w used in (3.20) and agree well with simulations over a range of N_b and η.

3.2 Simulations

The analytical model was developed assuming small numbers of co-site interferers and used an approximation for the distribution of the matched filter output for random pulse arrivals. These assumptions were compared to simulations using the same chip and filter characteristics described in Section 3.1. To be consistent with the model, a pulse lim-

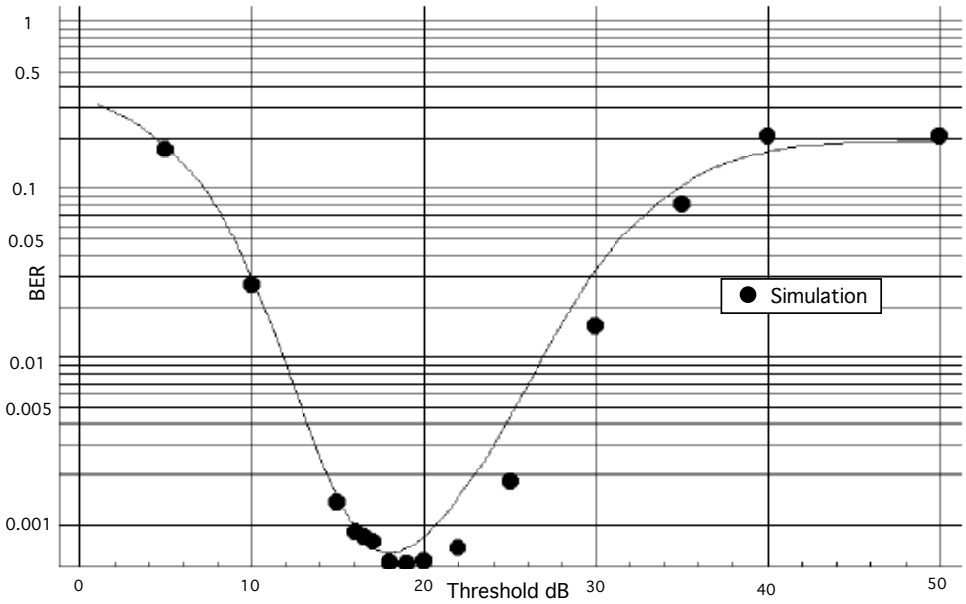

Figure 3.4: Threshold optimization range for 10 co-site interferers with received levels 40 dB above the background. A 10^{-3} BER performance is maintained for a discrimination threshold of 18 dB.

ited environment of 5200 simultaneous equal power users employing a binary offset, 100 chip/bit modulation, and a frame duration of $T_f = 128$ ns is defined as the desired distant background. The chip filter window is $\tau_{mf} = 1.2$ ns for this pulse width. Under these ideal equal power conditions the BER is less than 10^{-3}. However, past simulations have shown [27] that only a few relatively powerful uncoordinated near interferers can significantly degrade the overall performance. Ten additional interferers at 40 dB above the other users are added to the environment. Both the model and the simulation are evaluated for this case varying the chip discrimination threshold from zero to 50 dB. Not only does the model reasonably agree with the simulation in Fig. 3.4 but an appropriate selection of a chip discrimination threshold keeps the performance metric below 10^{-3} with the strong interferers. It is easy to see that in the limit, as the threshold becomes large, the BER metric significantly degrades just as a system without chip discrimination or coordinated blanking would. This isolation from strong IR interference comes with a small reduction in SNR, since a few chip/bit are discarded, but much of the potential interfering noise has also been eliminated.

If we take the same model for a number of interference levels, as in Fig. 3.5, it becomes clear that the optimum threshold range increases as I/S increases. Not only does this reduce the tracking tolerance on the threshold but because near chip collisions are more reliably discarded the BER floor performance improves. In addition the selection of the discrimination threshold becomes less critical for very powerful interferers as seen by the increasing threshold range at the lower BER floor. This simple threshold discrimination technique obviously performs better when there is a large near to far power discrepancy but that is precisely where the discrimination is really required. The lower power pulse collisions may not be thrown out as reliably by the discriminator but then they also contribute less degradation to the overall performance.

With an appropriate threshold and large near/far ratios the discriminator approaches the performance of perfect blanking. Using the blanking model developed in section 3.1.3 and comparing to chip discrimination simulations, Fig. 3.6 shows that at a near/far ratio of +80 dB performance is equivalent to that of a perfect blanking receiver. The equivalent blanking window used in (3.22) is determined to be $\tau_w = 1.41$ ns for a binary offset correlation response width of 1.2 ns. Performance of the chip discriminator is actually better for powerful interferers as compared to the same simulation with a 40 dB near/far ratio because of the more reliable discrimination. The analytic solution for perfect blanking then can be used to predict the BER floor seen in Fig. 3.5. Analytic solutions at lower interfering ratios and arbitrary thresholds are more approximate because of the matched filter pulse characteristic modulated by the stochastic nature of randomly timed pulse collisions.

Holding the threshold for discrimination at the optimum 18 dB level for the dense user case, the dependence on the near to far ratio can be seen in Fig. 3.7 where the power of the ten interfering sources is varied. The BER floor represents the performance for the equal power background case only. The ability of the discriminator to discard compromised chips does not occur until the interference power exceeds 20 dB. Beyond this point however, the discriminator successfully optimizes the performance by discarding the suspect chips and resolving the bit decision based on the surviving chips in that bit interval. The reduction in performance seen in Fig. 3.7 relative to the BER floor for the discriminator is due to the resulting reduced number of chips/bit at the decision. Never the less, this marginal reduction in performance is insignificant in comparison to the system performance without

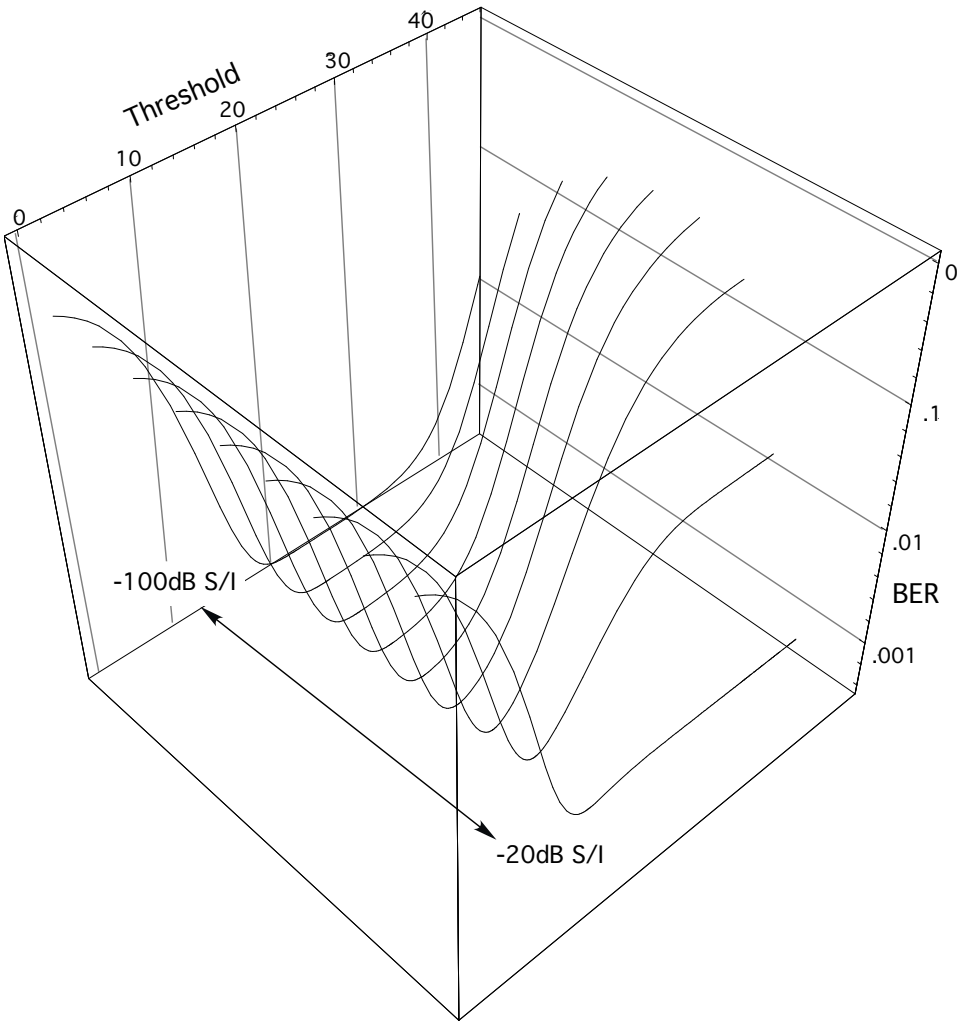

Figure 3.5: Optimum threshold discrimination range becomes much wider reducing the tolerance on the threshold value for larger interference levels. The optimum threshold remains constant over the interference range for constant background noise.

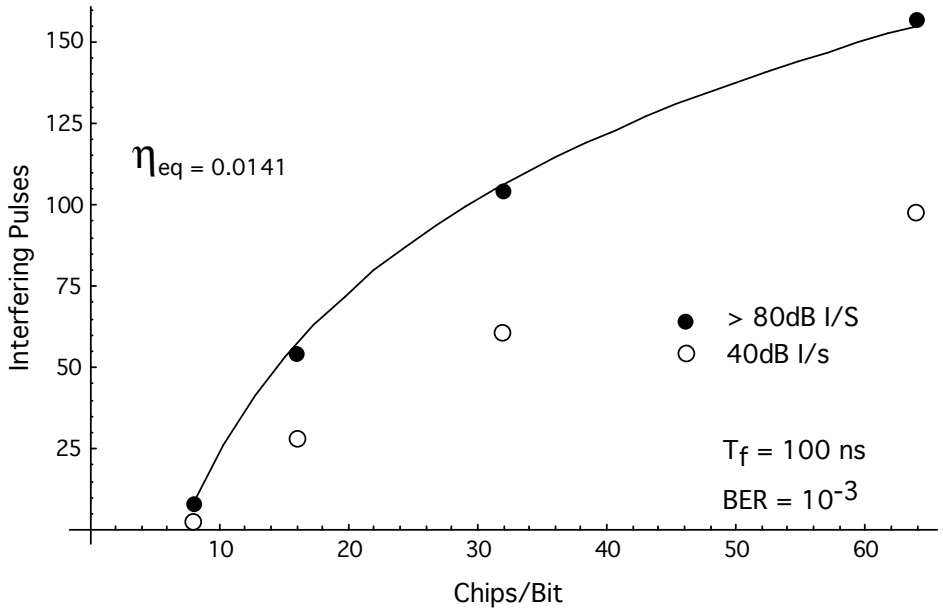

Figure 3.6: Comparison of analytic solution for perfect blanking to IR simulations using chip discrimination. High near/far ratios approach perfect blanking performance.

chip level discrimination. The discrimination performance actually improves slightly for very high levels of interference since compromised chips are discarded more reliably.

The chip by chip discrimination allows IR to use available excess bandwidth, in terms of chips per bit, to better tolerate co-site interferers. As an example of this concept, a simulation with the same system parameters is used with only 1000 equal power users reducing the ambient pulse noise floor. Assuming a pulse limited environment, the performance is quite good. However when additional co-site interferers at +40 dB are added, as shown in Fig. 3.8, the performance of the non-discriminating receiver significantly degrades with as few as one or two interferers. Alternatively the chip level discriminator, with a threshold set at 9 dB, can accommodate up to 100 co-site interferers while maintaining a reasonable BER performance metric.

Co-site interference of high throughput transponders can be of greater concern due to the sizable pulse density. Consider the number of 10 Mbit channels supported in a pulse limited environment where one of the 10 Mbit transponders is 80 dB above the background transmitters. Again using the same pulse characteristic defined in Section 3.1 for an opti-

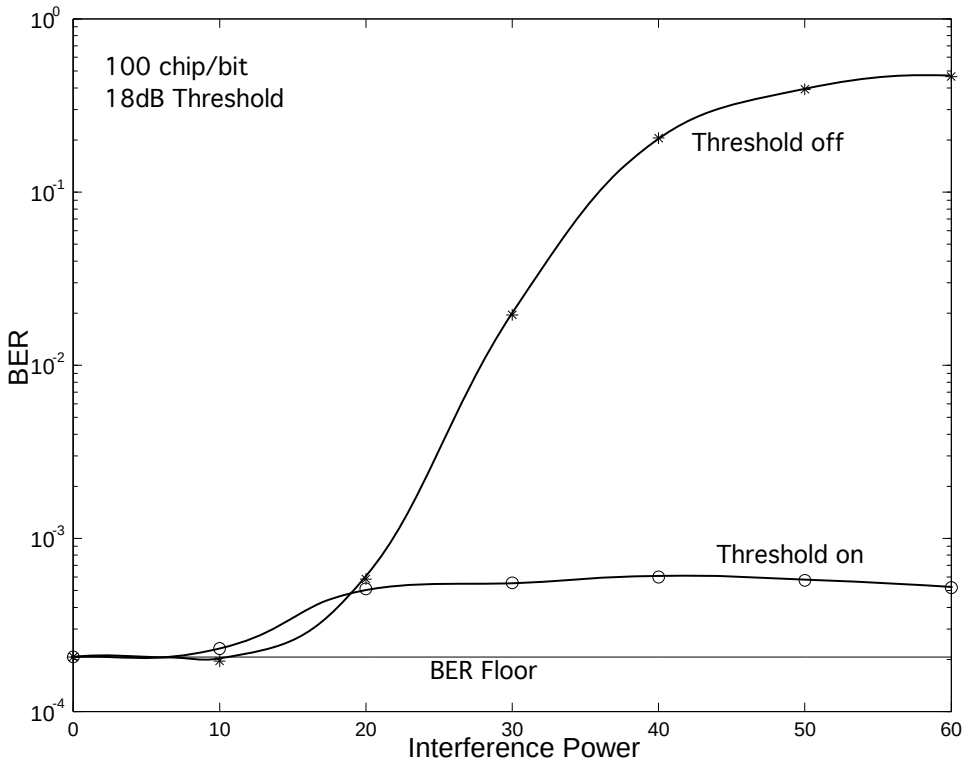

Figure 3.7: The linear correlation receiver performance without chip discrimination degrades rapidly with increased interference power relative to the optimum chip discrimination case. The marginal performance degradation of the chip discriminator relative to just background interference is due to a small number of discarded chips.

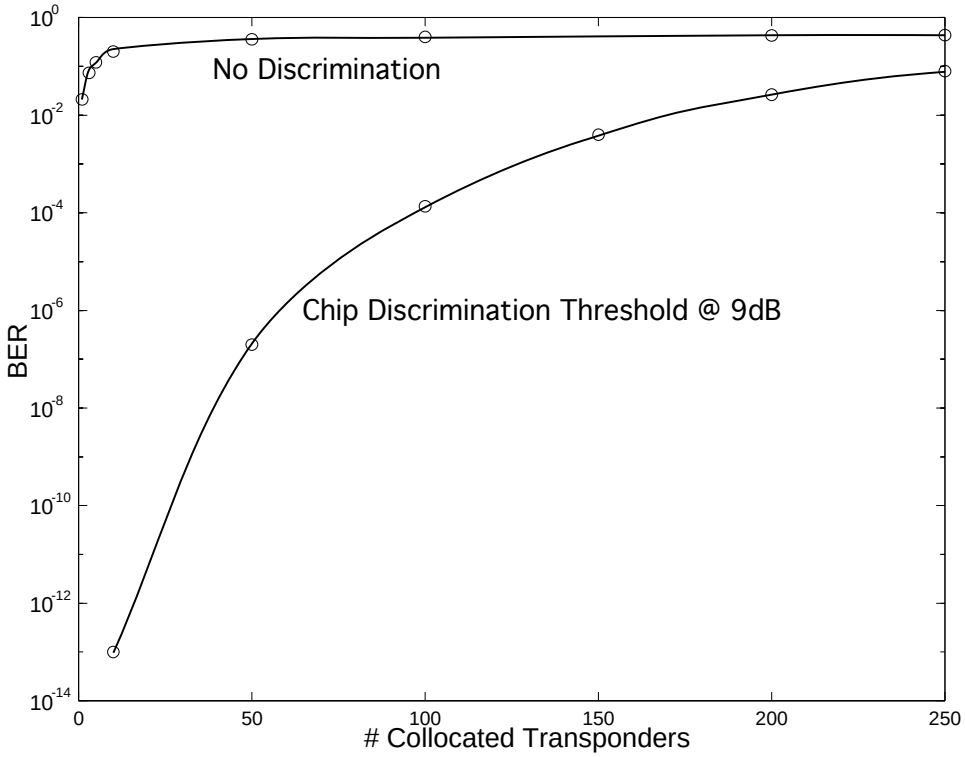

Figure 3.8: A linear correlation receiver without chip discrimination loses nearly all BER performance margin with as few as ten +40 dB co-site interferers even when equal power background interference is limited to 1000 users. In contrast the chip discriminator maintains much of the BER margin for a larger number of powerful interferers.

mum discrimination threshold and a frame time of $T_f = 100$ ns. The number of supported 10 Mbit channels is shown in Fig. 3.9 as a function of chips/symbol with the required BER in all cases below 10^{-3}. The curve indicates that the chip discrimination receiver performs better when there is an excess of chips/symbol, and appropriate multiplexing to maintain the bit rate, to favor in the decoding process. At some point the pulse density for a given number of users and chip rate exceeds a reasonable background interference and performance again declines.

Chip discrimination is certainly not limited to binary PPM but can be applied to higher order modulation indices such as M-ary PPM. Fig. 3.9 again considers the number of supported 10 Mbit transponders for an orthogonal 4-ary PPM modulation. The 4-ary modulation scheme supports more users as noted in [6], but also benefits from chip discrimination at the symbol decision. The binary offset and orthogonal PPM systems are both optimum near 8 chips/bit with the degraded capacity slightly less for the 4-ary case.

A hard limiter was suggested in [27] to optimize performance without power control. A comparison of hard limiting and chip discrimination for multiple binary offset PPM with a 10 Mbit data rate was simulated to illustrate the advantage of discarding excessive interference. Fig. 3.10 shows the number of supported 10 Mbit users for varying interference levels of a single interferer using 8 chip/bit in $T_f = 100$ ns frames. For a strong co-site interferer the chip discrimination receiver is more than double that of the resulting capacity of the hard limiter. As noted earlier, the chip discriminator performance is actually better where the strong interferer power makes discrimination more reliable. However, even with relatively lower power interferers of ~ 20 dB the linear receiver characteristic of the chip discriminator improves performance over the hard limiter equivalent.

3.3 Conclusions

A simple chip discrimination technique for use with Impulse Radio was presented that significantly improves bit error performance for a linear matched filter correlation receiver with large near to far power ratios. An analytical model is developed that estimates the BER performance for binary PPM impulse radio for varying S/I ratios and discrimination thresh-

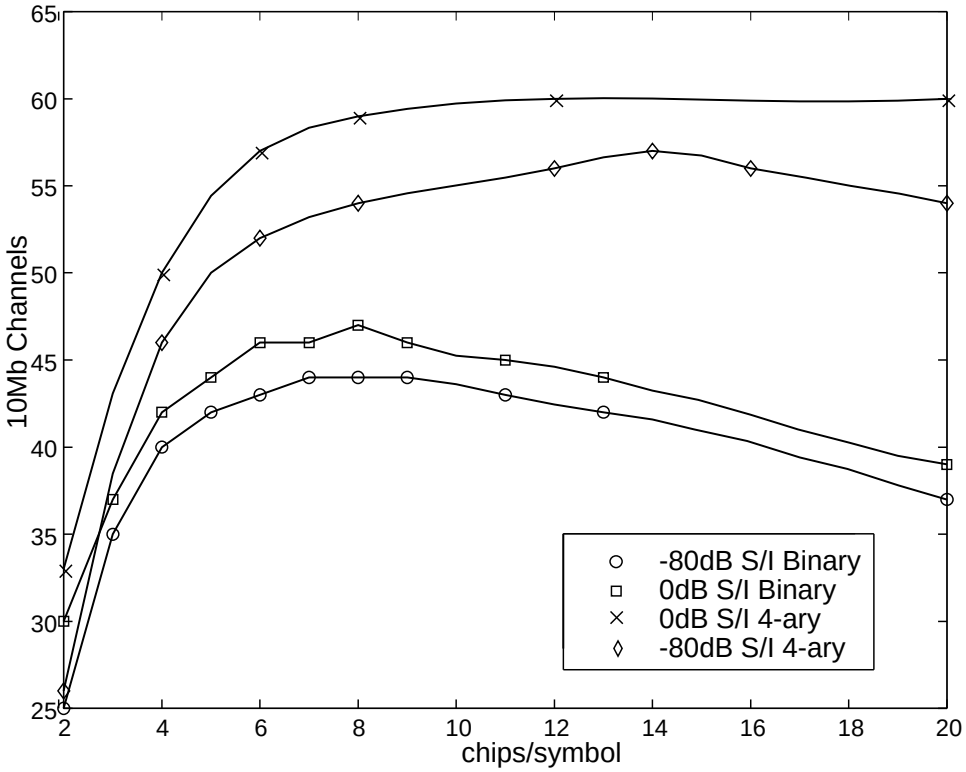

Figure 3.9: A comparison of binary offset and orthogonal 4-ary PPM responding to a single +80 dB 10 Mb random interferer. The optimum number of chips/bit required to maintain the greatest number of 10 Mb equal power users is nearly equal at $\sim$ 8 chips per bit.

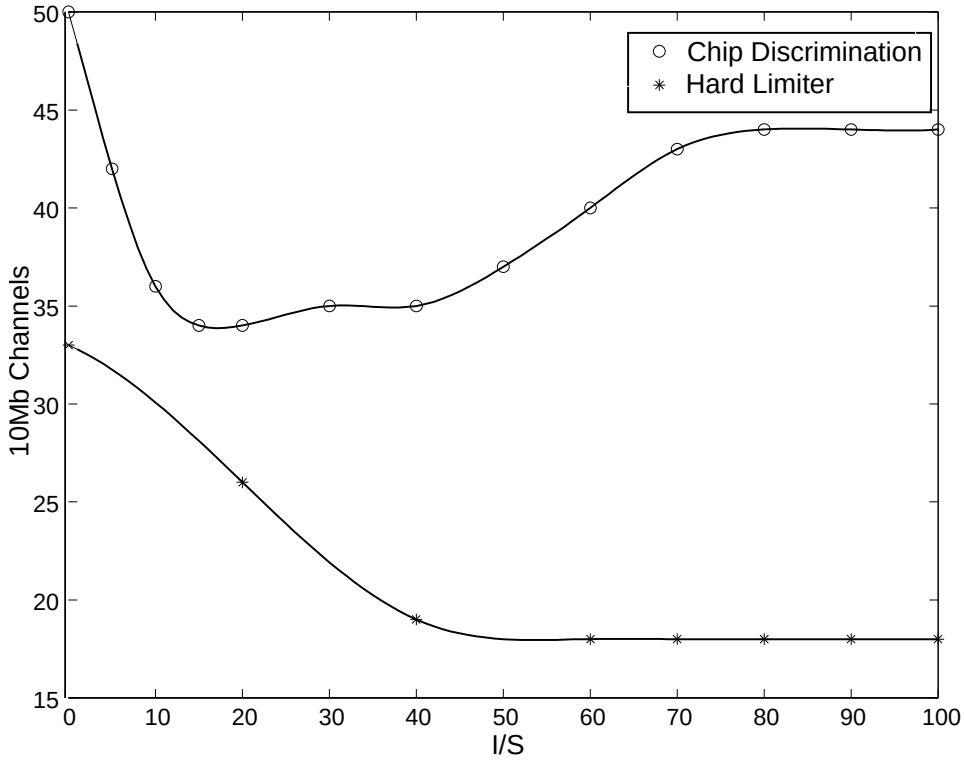

Figure 3.10: Chip discrimination for a linear binary offset PPM receiver as compared to a hard limited receiver with increasing interference power from a single 10 Mb source. The chip discriminator maintains a greater number of equal power 10 Mb users below a 10^{-3} BER performance.

olds. Both the model and simulations illustrate how performance loss in large interfering environments can be greatly reduced by selectively eliminating corrupted chips from the bit decision sum. Results show substantial improvement using this method for near interferers with I/S power ratios greater than 20 dB. Comparisons with perfect chip blanking solutions show good agreement for very large near/far power ratios. The discrimination technique can also be applied to M-ary modulation when multiple chip/ symbol modulation is applied. Simulation of binary offset PPM and 4-ary modulation with 10 Mbit channels illustrates capacity reduction with a single, uncoordinated interferer. The same binary offset PPM case is compared to a hard limiting receiver illustrating the combined advantages of chip discrimination in a linear receiver architecture.

Chapter 4

Rate Control with Chip Discrimination

A fundamental concern of any ad-hoc network is the mitigation of potential near/far power disparities. There is extensive literature on this issue in *narrowband* ad-hoc networks. For ultra-wideband (UWB) networks, complex power and rate control schemes have been proposed [34] but can not completely mitigate physical near/far transponder dispositions.

UWB offers the ability to transmit very narrow pulses, resulting in a low duty cycle communications scheme that provides opportunities for interference mitigation not possible in narrowband modulation schemes.

One approach is the chip discrimination technique presented in Chapter 3 and [36], that takes advantage of the low duty cycle nature of UWB to selectively and passively blank large interfering pulses from bit decisions. The technique exploits the fact that by using a large number of pulses (chips) per bit, the loss of a few chips/bit that result from occasional collision with large interfering pulses will have minimal impact on the resulting bit error rate. This simple method of using the remaining chips/bit from a UWB low duty cycle packet collision shows how excess bandwidth, in terms of chips/bit, can be used to defend against near pulse interferers. This technique alone provides substantial immunity from powerful near/far power ratios and is very simple to implement. Furthermore, chip discrimination can easily be added to a power or rate control protocol if desired.

The potential dynamics of an ad-hoc network with high near/far power ratios and dynamic or bursty transmissions make selection of an appropriate chip per bit rate, N_s, uncertain. Detecting or estimating unknown or uncoordinated near pulse interferers can be a receiver intensive task if relative timing relationships are not known *apriori*. In this chapter, a technique is presented for dynamically adjusting the number of chips/bit to maximize throughput. The technique builds on chip discrimination, and also exploits the low duty cycle nature of UWB radio.

The rate control method keeps this estimation process simple by using the chip discrimination logic described in Chapter 3. The technique assumes single pulse detection per chip frame interval, T_f, as is typically done with impulse radio [4, 7, 50, 27]. The method adds to this a chip discrimination threshold from which a stochastic estimate of near pulse interference can be derived. The number of chance pulse collisions that result in chip threshold exceedance over a given number of chip frames is used to determine the minimum number of pulses, N_s, required to maintain a desired bit error performance.

The estimation of the near-pulse interference and selection of the required chip rate is proposed here as one component of a MAC layer protocol in a peer-to-peer configuration. The combined use of chip discrimination with the relatively simple addition of estimating local pulse interference to set N_s in a MAC layer provides a more robust receiver in co-site settings. The combination also optimizes the data throughput for a fixed peak and average power link. Such a throughput adaptation would benefit most from environments with high near/far power ratios and dynamic or bursty transmissions, taking advantage of relatively idle periods of interference.

An understanding of chip discrimination given in Chapter 3 is required since many of the features for the rate control concept are derived from it. The following sections provide the system model and description for an adaptive rate control technique applied to a packet queue transponder. Simulations of varying pulse density environments applied to a single peer-to-peer link employing chip discrimination and rate control are presented in section 4.2.

4.1 System Model

The environment considered is a single hop packet transmission link with a background of similar uncoordinated transponders uniformly distributed in area. Each transponder operates at the same peak and average power using autonomous chip discrimination. There is no assumed power control other than the peak and average power limitation. A transmitter assigns a chip/bit rate N_s for each packet based on a required bit error rate performance at the receiver. Since the transponder is assumed limited in peak and average power the peak data throughput is inversely proportional with the selection of N_s and the chip frame rate T_f. An individual receiver may experience varying degrees of background pulse interference from the aggregate population as well as potential near or co-site interferers. The pulse limited environment of a large number of transponders in a given area will tend to produce a relatively stable interference floor at the receiver. The closest of these neighboring transmitters will greatly influence the SNR performance. The receiver will track and set a threshold for chip discrimination to limit strong pulse collisions for these closest of transmitters. A fixed, or relatively slowly varying, fixed chip per bit transmitter would be limited to selecting N_s for the worst case interfering packet transmission scenario. A MAC layer component is described here that can quickly adapt each transmitted packet to near current interference conditions and consequently optimize throughput on the link.

4.1.1 MAC Layer Rate Control

During packet transmission a receiver using chip discrimination rejects select chips that exceed a given threshold when chance pulse collisions occur from near or co-site transmitters. Not only does this selective elimination of interference pulses from the bit decision sum help BER performance in dense powerful pulse interference cases but gives an indication of the current co-site pulse density. A receiver, either actively receiving a packet or idle, can continue to record the number of frames T_f where the chip threshold is exceeded. In this case, to keep the receiver simple and the potential receiver current low, a single chip receive interval is observed in each frame time T_f. In this case a receiver continuously records the number of threshold exceedances over the last N_i frames. The selection of N_i

may depend on the bursty nature of the interference. If N_i is too short the uncertainty of the estimate will be large. Alternatively if N_i is too long the adaptive rate of the transmitter may be too slow.

The MAC layer component begins with a packet transmission request from either the receiver or transmitter. On request, the receiver uses the most recent chip erasure count N_X from the last N_i frames to determine the minimum chip rate N_s required to sustain the requisite BER performance. On receipt of this information the transmitter will immediately begin the packet transmission at the requested chip/bit rate. Since this is a passive estimate of the local interfering transmitters there is of course a chance for near packet transmissions starting during our transmission. Unlike narrowband packet collisions, the chance collisions of UWB chip pulses is mitigated partly by hopping codes and potentially eliminated by chip discrimination. After packet transmission the receiver acknowledges packet success or failure. If the packet transmission failed the transmission would be attempted again using the same sequence described above and the most recent erasure count N_X partly determined during the failed packet attempt.

Variations on this protocol for multiple packet transfer can be adapted to include the threshold exceedance count in the packet status acknowledge allowing continuous packet transmission with packet reordering at the receiver.

4.1.2 Packet Queue

The variable rate performance is evaluated by observing the input packet queue statistics of a transmitter operating in a bursty environment with a high near/far power ratio at the receiver. The transmitter has a single packet queue with a Poisson packet arrival rate. All packets for this analysis are assumed equal size and transmitted, first in first out (FIFO), immediately upon arrival. For the case of a fixed N_s, normally assumed [13, 31, 4], the performance can be compared to that of a $M|D|1$ queue. For a fixed N_s and T_f rate the generating function for the error free queue can be found in [52] as:

$$G_n(z) = \frac{(1-\rho)(z-1)}{[\, z\, e^{\rho(1-z)} - 1\,]} \tag{4.1}$$

Where ρ is the ratio of the offered load λ in packets per second in this case to the link transmission rate μ. The adaptive rate algorithm used here will not have a constant transmission rate but can be compared to an equivalent average fixed rate link by deriving the queue occupancy probabilities through successive differentiation of the generating function with $p(3)$ as an example given in (4.3).

$$p(n) = \frac{1}{n!} \frac{d^n G_n(z)}{dz^n} \bigg|_{z=0} \tag{4.2}$$

$$p(3) = (\rho - 1)(e^{\rho} - 1 - \rho)e^{\rho} \tag{4.3}$$

Then comparing simulation histograms of a sample link queue to the accumulated state probabilities defined as:

$$P(N) = 1 - \sum_{n=0}^{N} p(n) \tag{4.4}$$

Even with a variable rate MAC layer protocol described in section 4.1.1 and a dynamic pulse interference environment, the average queue occupancy will have the same exponential characteristic as an equivalent error free $M|D|1$ curve derived from (4.4) for an appropriate selection of ρ. The simulation results are compared to theoretical and simulated fixed transmission rate UWB links to illustrate the tradeoff between packet loss and transmission time in dynamic pulse environments.

4.2 Simulations

To gain some insight with all the stochastic components of the environment and the nonlinear nature of chip discrimination several simulations were constructed. The UWB adaptive rate MAC technique was evaluated in a bursty environment using binary offset modulation and a matched filter receiver [4, 5, 13] with a pulse time scale coefficient $t_n = 0.29$ ns. The relative locations of the interfering transponders bounded by a 200 meter radius are show in Fig. 4.1 for one case with the observed test receiver at the origin. Within this pulse

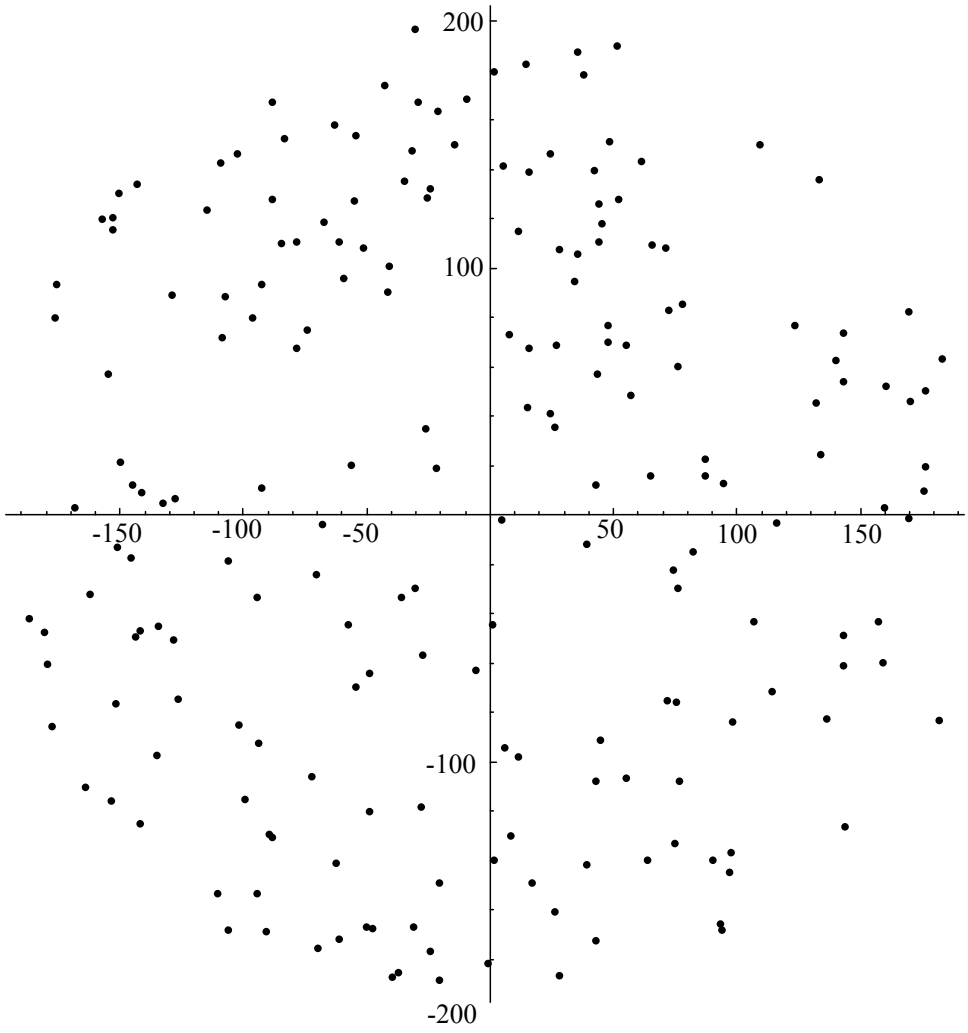

Figure 4.1: Uniform spacial transponder distribution used for simulation.

density we neglected thermal noise. All transponders in this volume are equal power with a 4^{th} power spacial path loss. All interfering sources are modeled assuming independent hop codes with uncorrelated packet generators. Additional large bandwidth, co-site interferers are added to show how the receiver adapts to a dense environment. Parameters for the area and co-site interfering sources are listed in Table 4.1.

The desired test link from a transmitter at 100 meters has a chip frame time T_f = 100 ns for a peak throughput of 10 Mcps. Chip discrimination is used to limit the near power interference. The input to the test link queue is 5 kbit packets at a Poisson rate λ_1 = 250 per second for an average throughput of 1.25 Mbps. The transmit link would just meet this capacity at 8 chip/bit. A packet is retransmitted if there are 5 or more bit errors for a BER of $\leq 10^{-3}$. The receiver also continuously records the number of chip erasures over the last 500 μs resulting in 5000 samples at the T_f rate. When a packet transmission is requested the receiver uses the reported erasure rate N_X for the last 500 μs with the thresholds listed in Table 4.2 to determine the required chip/bit rate. This chip rate is then passed on to the transmitter. For this simulation the MAC layer messaging is assumed error free and without delay.

Simulations were run with transponders randomly distributed in the volume shown in Fig. 4.1. The cumulative packet queue occupancy probability as described by (4.4) is plotted in Fig. 4.2 for this case. First it should be noted that a linear matched filter receiver without chip discrimination would not perform well at all in this dense environment. With 4 chips/bit and discrimination enabled the link easily maintains throughput with virtually no packet failures. With the same link limited to 3 chip/bit the packet failure rate is 6%. The adaptive rate algorithm selected 3 chip/bit for packet transmission 79% of the time with less than 3% packet failure. The attempted risk of transmitting at 3 chip/bit with detected light interference is a trade between higher throughput and potential retransmission. Under these conditions the adaptive rate algorithm resulted in equivalent optimum throughput to the fixed 4 chip/bit link but with 18% fewer pulses required.

The benefits of chip discrimination [36], and in this case pulse interference detection, are more pronounced when near/far power ratios become large. We now apply the co-site interferers listed in Table 4.1 to the distributed sources. Four of these co-site sources generate independent 5 ms packets of 500 k pulses each. The ability to reliably detect

Table 4.1: Simulation Environment Interferers

Number	λ	T_f	N_s	**Packet Size**	**Location**
200	30	100 ns	8	5k	Uniform Area
4	50	10 ns	2	250k	co-site 100 dB
1	35	100 ns	8	5k	co-site 100 dB

Table 4.2: Chip Rate Thresholds for 0.5 ms Exceedance Rates

Chip/Bit	**Exceedance Count** N_X
3	$0 \leq 200$
4	$201 \leq 580$
5	$581 \leq 1000$
6	$1001 \leq 1400$
7	$1401 \leq 1700$
8	> 1700

interferers allows the adaptive rate algorithm to take advantage of the idle packet periods to reduce N_s. The resulting throughput shown in Fig. 4.3 for the adaptive rate algorithm exceeds any of the fixed N_s links. The effective $M|D|1$ throughput for the variable rate case is $\rho = 0.7625$ for an equivalent error free data rate of 1.64 Mbps. The best fixed rate link at $N_s = 6$ chip/bit effectively produced an error free data rate of 1.5 Mbps. The adaptive rate algorithm also accomplished this throughput with 8.4% fewer pulses after accounting for packet retransmission rates and the relative chipping rates the adaptive algorithm selected listed in Table 4.3. Selecting N_s involves the tradeoff between the re-transmission rate and the transmission time. The fixed 5 chip/bit link shown in Fig. 4.3 falls off due to packet failure rates. Alternately a 7 chip/bit link shown in Fig. 4.4 will have a much lower packet failure rate as noted by the theoretical 7 chip/bit $M|D|1$ error free performance curve. But the packet transmission time adversely affects the queue load resulting in little advantage. The combination of chip discrimination and this adaptive rate control with fast estimation of pulse interference yields an efficient link throughput.

Table 4.3: Relative Chip Rate Selection

Chip/Bit	Packet Rate Averages
4	33 %
5	22 %
6	24 %
7	17 %
8	4 %

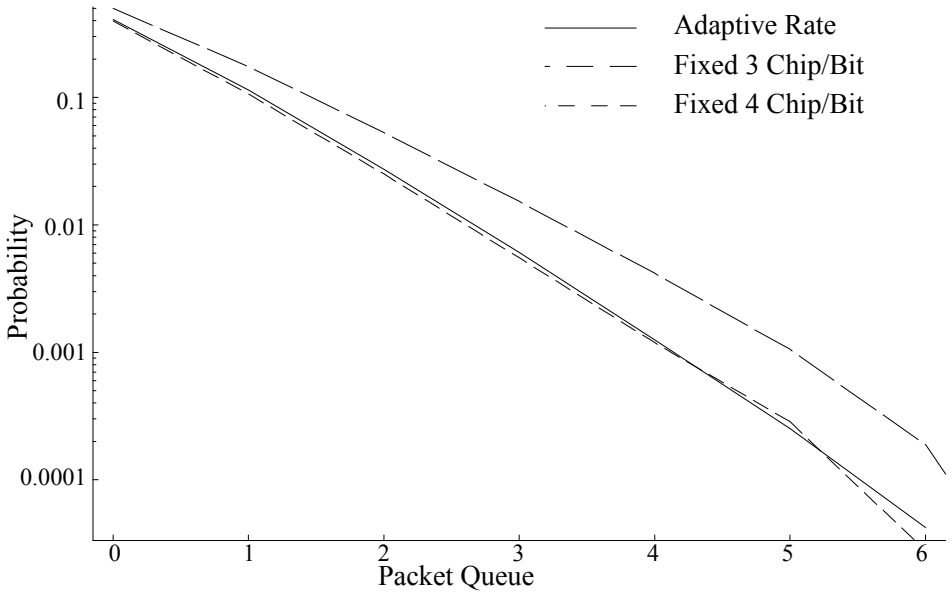

Figure 4.2: Performance without co-site interferers. Adaptive rate algorithm selects 3 chip/bit 79% of the time yet meets 4 chip/bit performance with 18% fewer pulses.

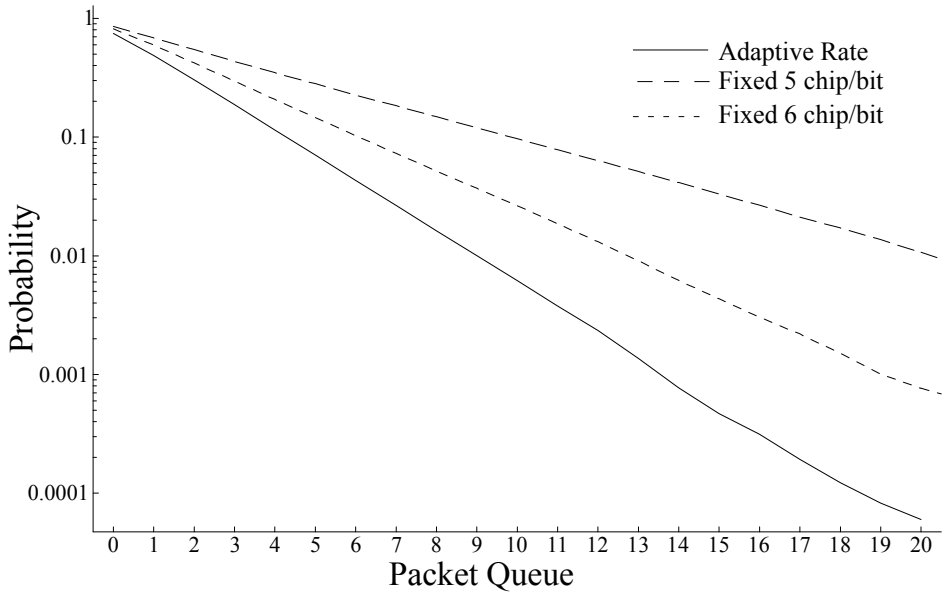

Figure 4.3: Performance with all interferers listed in Table 4.1. None of the fixed N_s links match the ability of the adaptive rate link to clear the queue.

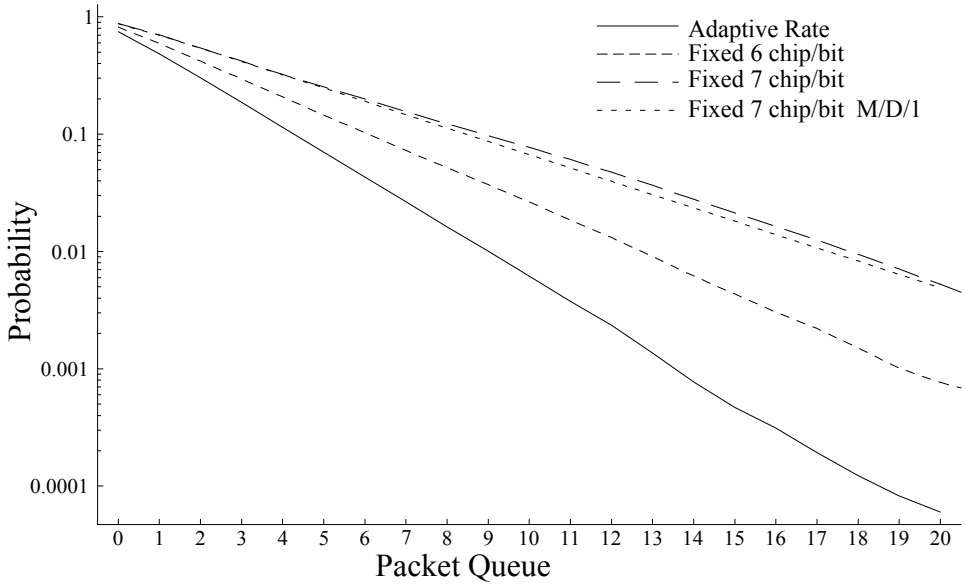

Figure 4.4: Seven chip/bit is nearly error free as compared to the theoretical $M|D|1$ performance but extends transmission time.

4.3 Conclusions

In this chapter, a technique was presented for adjusting the number of chips/bit to maximize throughput. The technique builds on chip discrimination, exploits the low duty cycle nature of UWB radio, is very simple to implement, and uses only locally derived data. The efficacy of this method is demonstrated using simulation in bursty, pulse limited environments. The technique demonstrates improved throughput compared to fixed parameter links and equivalent theoretical $M|D|1$ queues. This performance was also achieved with an overall average reduction in required transmitted pulses.

Chapter 5

Estimation of Packet Success with Individual Pulse Blanking

In previous work we have shown how chip (pulse) discrimination [36] can be used to adapt a UWB chip per bit rate [38] to optimize throughput under conditions of large near-far power ratios. As indicated before, a fundamental concern of any ad-hoc network is the mitigation of potential near/far power disparities. There is extensive literature on this issue for *narrowband* ad-hoc networks [53, 54]. For ultra-wideband (UWB) networks, complex power and rate control schemes have been proposed [34] but can not completely mitigate physical near/far transponder dispositions. Theoretical capacities of UWB systems [4, 7, 50, 55] typically assume identical receive powers for all users. However pulse collisions where near far power ratios are large can greatly limit performance and capacity for UWB. The unique potential for covert operation and dynamic bandwidth for impulse radio can be difficult to obtain without due attention to these issues. The especially harsh requirements of a tactical environment place limitations on physical separation adding increased complexity to network distribution.

The technique presented in [36] takes advantage of the low duty cycle nature of UWB to selectively and passively blank large interfering pulses from bit decisions. The tech-

nique leverages the use of a large number of pulses (chips) per bit to mitigate the loss of a few chips lost from occasional collisions with large interfering pulses. This minimizes the impact on the resulting bit error rate. This simple method of using the remaining chips/bit from a UWB low duty cycle packet collision shows how excess bandwidth, in terms of chips/bit, can be used to defend against near pulse interferers. This technique alone provides substantial immunity from strong near/far power ratios and is very simple to implement. Furthermore, chip discrimination can easily be added to a power or rate control protocol if desired.

We extended this technique in [38] where we presented a method for adjusting the number of chips/bit to maximize throughput. This is desirable where the dynamics of a tactical ad-hoc network with high near/far power ratios and dynamic or bursty transmissions make selection of an appropriate chip per bit rate, n_i, uncertain. The technique is built on chip discrimination, exploiting the low duty cycle nature of UWB radio. Our method adapted the chip discrimination threshold to determine a stochastic estimate of near pulse interference. In effect, the number of chance pulse collisions that result in chip threshold exceedance over a given number of chip frames was used to determine the minimum number of pulses, n_i, required to maintain a desired bit error performance. The estimation of the appropriate chip rate n_i in this case was quantitatively determined through simulation trials.

This chapter develops a theoretical basis for the probability of packet loss using this variable rate technique and pulse discrimination. The algorithm provides a rapid method for determining an optimum chip per bit rate table for assumed packet interference conditions. As a first order simplification in the development of this probability, we assume that the near interfering pulses are reliably detected when they collide and result in the deletion of the pulse from the bit decision sum. The result of any chip discrimination process is variable SNR conditions based on lost signal power as well as noise variation. Additionally any portion of a desired packet can experience varying degrees of packet interference based on random overlapping events as exemplified in Fig. 5.1.

Regardless of the unique interfering case, we define the success of a given packet based on a maximum number of allowable bits in error. No other error correction coding is assumed here and all bit positions in the packet are of equal value. However other practical implementations would likely acknowledge the better immunity protection found for bits

in proximity of the interference estimation period and prioritize value appropriately. Unlike other complex methods for evaluating packet error for overlapping cases [40, 56] we find that reasonable accuracy and simplicity can be maintained by quantifying the average portion of packet interference levels. The proportion of the packet affected by the varying degrees of interference change conditionally based on the number of known interferers at the beginning of the packet. The chip per bit rate selected is also based on the number of detected interferers.

In section 5.1 we develop an algorithm for determining the probability of average packet failure for a Poisson packet interfering model. The ideal optimized metric of a peer-to-peer packet queue link, is the effective channel packet throughput. Constrained to a maximum pulse transmission rate and fixed packet data size, the selection of an appropriate chip per bit rate becomes a trade between packet success and transmission time. The aggressive reduction of bit pulse coding at the risk of packet loss and retransmission during anticipated periods of low interfering levels can be as important as robust pulse coding selection for high levels of interference.

The advantage of a computationally simple theoretical method for estimating packet success probabilities and average bit pulse rates allows for optimization analysis of the rate selection table. Parametric considerations for background noise, pulse framing rates, interference characteristics, and pulse widths can then be applied to practical implementations. Detecting or estimating unknown or uncoordinated near pulse interferers can be a receiver intensive task if relative timing relationships are not known *apriori*, as they are assumed here. However, the results we theoretically derive here can be applied to the proposed rate control method in [38] using autonomous pulse exceedance rates as a first order estimate of interference levels.

Simulations of varying pulse density environments applied to a single peer-to-peer link employing chip discrimination and rate control are presented in section 5.2. The results show good agreement with the theoretical prediction of packet success rates for varying rate tables. Throughput comparisons are also shown illustrating the advantage of adaptive rate control. Optimization of the required chip per bit rate for these simulations was verified using the theoretical basis described here.

5.1 System Model

For a theoretical bound on adaptive rate control with individual chip discrimination we assume that pulse collisions are always detected and discarded from the bit decision sum. The desired packet transmission assumes single pulse detection per chip frame interval, T_f, as is typically done with impulse radio [4, 7, 50, 27]. The number of interfering packets are also assumed known just prior to packet transmission. The chip per bit rate selected by the receiver and used by the transmitter as part of a MAC layer protocol is based on the number of interfering packets detected at the receiver as illustrated in Fig. 5.1. For our notation here the number of chips per bit for a given number of interferers is n_i where i is the number of interferers. The resulting rate control table is defined below in equation (5.1) as:

$$\Delta_k = \begin{pmatrix} n_0 \\ n_1 \\ \vdots \\ n_k \end{pmatrix} \tag{5.1}$$

The chip per bit rate selected at the beginning of the packet transmission is maintained until the end of the packet. However the number of interfering transmissions may vary during this packet transmission and may not be commiserate with the estimate of the number of interferers detected at the beginning. The example shown in Fig. 5.1 illustrates a case where two interferers are detected at time 0 while only a fraction of the packet experiences two interferers and the remainder have only a single blanking interferer. The resulting success or failure of the desired packet is determined in part by the anticipated portion the desired packet overlaps $0, 1, 2, \ldots$ interferers. Other factors are the chip per bit rate selected, background SNR, pulse width and chip frame times.

For this analysis [57] we consider the resulting average degree of interfering packet overlap for y interferers of duration L having identical independently uniformly distributed start times in the interval $[-L, L]$. The longest duration of the desired packet transmitted is also L for the maximum chip per bit rate in Δ_k. For an arbitrary time $\alpha, \alpha \in [0, L]$, we consider the probability of a given number of interferers that change state, either turning off or turning on. Defining the differing event probabilities for an interfering packet changing

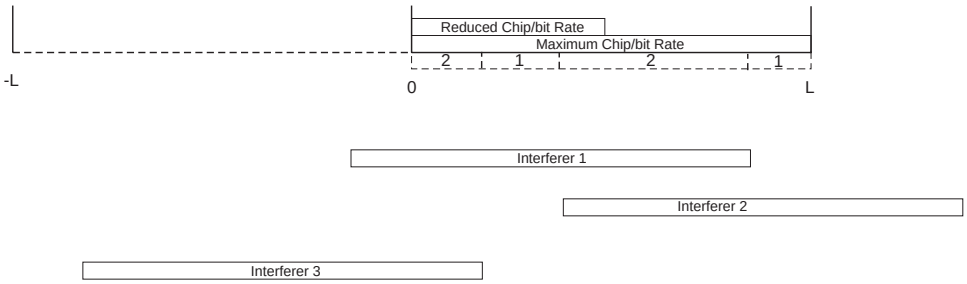

Figure 5.1: Illustration shows the relationship between interfering packets and varying degrees of overlap. Chip rate selection is determined by the number of overlapping interferers at time 0.

state at time α

$$\begin{aligned} A &= Prob(\text{"}ON\text{"} \rightarrow \alpha | \text{"}ON\text{"} \rightarrow 0) = \frac{(L-\alpha)}{L} \\ B &= Prob(\text{"}OFF\text{"} \rightarrow \alpha | \text{"}ON\text{"} \rightarrow 0) = \frac{\alpha}{L} \\ C &= Prob(\text{"}OFF\text{"} \rightarrow \alpha | \text{"}OFF\text{"} \rightarrow 0) = \frac{(L-\alpha)}{L} \\ D &= Prob(\text{"}ON\text{"} \rightarrow \alpha | \text{"}OFF\text{"} \rightarrow 0) = \frac{\alpha}{L} \end{aligned} \tag{5.2}$$

we can combine the probability for a given number of interferers turning off and on at time α as:

$$\left(\frac{L-\alpha}{L}\right)^{A+C}\left(\frac{\alpha}{L}\right)^{B+D} \tag{5.3}$$

For a given number of interferers $y \in [-L, L]$ and conditioned on z known interferers on at time zero we define E as the number of interferers that do not change state.

$$\begin{aligned} E &= A+C \\ y-E &= B+D \end{aligned} \tag{5.4}$$

This leaves $y-E$ as the number that do change state. As noted earlier the chip per bit rate can vary with Δ_k based on z known interferers at time zero. This means the packet

transmission duration can vary for a fixed data packet size of N_b bits per packet. If we define the duration of the packet as a fraction $\Delta \in [0,1]$ of L and integrate over all possible values of α we can define the probability for a given E in equation (5.5)

$$g(y,E,\Delta) = \int_0^{\Delta L} \left(\frac{L-\alpha}{L}\right)^E \left(\frac{\alpha}{L}\right)^{y-E} \frac{1}{\Delta L}\, d\alpha \tag{5.5}$$

with evaluation and reduction to (5.6).

$$g(y,E,\Delta) = \sum_{i=0}^{E} -1^{E-i} \binom{E}{i} \frac{\Delta^{y-i}}{y-i+1} \tag{5.6}$$

Considering all the valid cases of E for a given number of interferers y with z on at time zero and x on at time α, it is easier to consider the number that change state ($F = y-E$). If both z and $y-z$ are greater than zero and x and $y-x$ are greater than zero, then in addition to the minimum $|x-z|$ required to satisfy the end conditions, one additional ON interferer can turn off with one off turning on in order maintain the end condition [57]. This continues until all of the on or off interferers are exhausted at the beginning or the end. The number of combinations of transitions is simply the product of the possible combinations of off to on transitions and the possible combinations of on to off combinations. The fractional portion of the desired packet with x interferers reduces to (5.7) with the coefficient $E = y-|x-z|-2k$ set in the generating function (5.6).

$$\begin{aligned} P_\delta(x|y,z,\Delta) = & \sum_{k=0}^{min(x,z,y-x,y-z)} \binom{z}{max(z-x,0)+k} \cdots \\ & \binom{y-z}{max(x-z,0)+k} g(y,y-(|x-z|+2k),\Delta) \end{aligned} \tag{5.7}$$

For a given number of interferers $y \in [-L,L]$ the probability of having z interferers overlap

at time zero is given by (5.8).

$$P_{b1}(z|y) = \binom{y}{z}\left(\frac{1}{2}\right)^{y} \tag{5.8}$$

This combined with the conditional overlap probability expression above allows us to define a set of probability matrices for each case of y interferers defined as $\Psi_{y,\Delta}$.

$$\psi_{x,z} = P_{b1}(z|y)P_{\delta}(x|y,z,\Delta) \tag{5.9}$$

$$\Psi_{y,\Delta} = \begin{pmatrix} \psi_{0,0} & \psi_{1,0} & \cdots & \psi_{y,0} \\ \psi_{0,1} & \psi_{1,1} & \cdots & \psi_{y,1} \\ \vdots & \vdots & \vdots & \vdots \\ \psi_{0,y} & \psi_{1,y} & \cdots & \psi_{y,y} \end{pmatrix} \tag{5.10}$$

Since we use the observed number of interferers z to select the chip per bit rate from (5.1) above we effectively have the fractional length Δ as well. The matrix in (5.10) now gives the fraction of the desired packet with x interferers as a function of the chip per bit rate selected by the receiver. Using a set of matrices $\Psi_{y,\Delta}$ for varying interfering densities can now be used to predict packet failure for alternative bit spreading rates in (5.1).

The fraction of N_b packet bits exposed to x interferers can be derived from (5.10) for all y and z cases. The fraction of the packet exposed to x interferers is now δ_x.

$$\delta_x = \frac{\Psi_{y,\Delta}(x,z)}{P_{b1}(z|y)} \tag{5.11}$$

We define the number of bits affected by x interferers as $N_b(x)$.

$$N_b(x) = N_b\ \delta_x \tag{5.12}$$

The bit error rate in a portion of the packet with x interferers is dependent on the number

of surviving chips as well as the background SNR. Assuming the interfering pulses are iid in a chip frame duration of T_f seconds the chip survival probability can be modeled as a binomial distribution. The probability that a single desired pulse correlation window is hit in T_f seconds, and therefore removed from the bit decision sum, is γ. For a possible n chips per bit, which is dependent on the rate table Δ_k used, the bit error rate can be defined as

$$\varepsilon_b = \sum_{i=0}^{n} \binom{n}{i} (1-\gamma)^{xi} (1-(1-\gamma)^x)^{n-i} \frac{1}{2} \operatorname{Erfc}\left[\sqrt{i \frac{s_c}{2\sigma_c^2}}\right] \tag{5.13}$$

for a given number x of like interferers.

In this packet based analysis we are concerned with the packet failure or retransmission rate in such an environment. The bit error rate ε_b is very sensitive to the number of interferers and a given packet can have varying proportions of interfering overlap as illustrated in Fig. 5.1. To determine the packet success rate we define the number of bits that can be in error for the packet size N_b and list the number of unique ways these bit error sums can occur for a given y interferers. For y interferers there are y regions of the packet with differing bit error rates. Each region on average has $N_b(x)$ bits, as previously determined in (5.5 - 5.12), that can be in error. The array Γ_y in equation (5.14) is the composition of bit errors for y regions of all bit error sums up to the maximum defined number of bit errors allowed in a packet.

$$\Gamma_y = \begin{pmatrix} \gamma_{0,0} & \gamma_{0,1} & \cdots & \gamma_{0,y} \\ \vdots & \vdots & \vdots & \vdots \\ \gamma_{\eta,0} & \gamma_{\eta,1} & \cdots & \gamma_{\eta,y} \end{pmatrix} \tag{5.14}$$

An example of such a composition of up to five bit errors for $y = 1$ interfering region is

shown below:

$$\Gamma_1 = \begin{pmatrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \\ 0 & 2 \\ 1 & 1 \\ \vdots & \vdots \\ 3 & 2 \\ 4 & 1 \\ 0 & 5 \end{pmatrix} \tag{5.15}$$

The bit error composition array has $y+1$ columns to include the region with no interfering packet overlap and has $C_k(n)$ rows for the composition of k into n parts.

$$C_k(n) = \binom{n+k-1}{k-1} \tag{5.16}$$

For each component of the packet with x interferers the probability of κ bit errors out of $N_b(x)$ bits is again a binomial probability

$$\mathbf{P}_{\kappa,N_b(x)} = \binom{N_b(x)}{\kappa} \varepsilon_b^{\kappa} \left(1-\varepsilon_b\right)^{N_b(x)-\kappa} \tag{5.17}$$

with the bit error ε_b as defined in (5.13).

For the cases analyzed here we assume a Poisson arrival rate for the interfering packets. Each interferer generates packets at the same average rate with all packets the same duration of L seconds. The probability of x interfering packets arriving within the desired packet window of $[-L,L]$ is now given given by:

$$P_x = \frac{(\lambda 2L)^x \exp\left(-\lambda 2L\right)}{x!} \tag{5.18}$$

An expression for packet success for a given interference level can now be provided here

$$\sum_{i=1}^{C_k(x+1)} \prod_{j=0}^{x+1} \mathbf{P}_{\Gamma_y(i,j),N_b(j)} \tag{5.19}$$

by applying $\mathbf{P}_{\kappa,N_b(x)}$ to a composition of acceptable bit error outcomes in Γ_x . But this success rate is influenced by the rate table (5.1) which is a function of the number of detected interferers prior to transmission. The rate table not only changes the bit error immunity but the transmitted packet length as well. The overall packet success rate can now be determined by accumulating the individual packet success probabilities from (5.19) weighted by the event probabilities for a given interference level x as defined in (5.18, 5.8).

5.2 Simulations

The algorithm described in section 5.1 can be used to quickly determine optimum rate table values for varying channel conditions. The optimization of the selected chip per bit rate for a fixed data length packet link has two components to consider. Assuming a packet retransmission requirement, there is a trade between reduced chip rates for shortened packet transmission time offset by increased bit error immunity. The reduced packet transmission time not only rapidly clears the transmit queue but makes better use of the *apriori* knowledge of the interference at the beginning of the transmission. Relatively longer packet transmissions may be more robust because of greater chip rates but benefit less from aging interference estimates prior to the transmission.

The received impulse used for simulation is the Gaussian mono-pulse as defined in [13] with shape factor t_n= 0.29 ns. We assume the hopping times are independent, identically distributed random variables, uniformly distributed over the frame with the pseudorandom hopping sequence length much larger than n_i. The asynchronous interferers transmission time offset relative to the desired signal are independent, identically distributed random variables, uniformly distributed over $[0, T_f]$. The accuracy of the algorithm as well as the advantage of adaptive rate control [38] were evaluated in a simulation of varying degrees

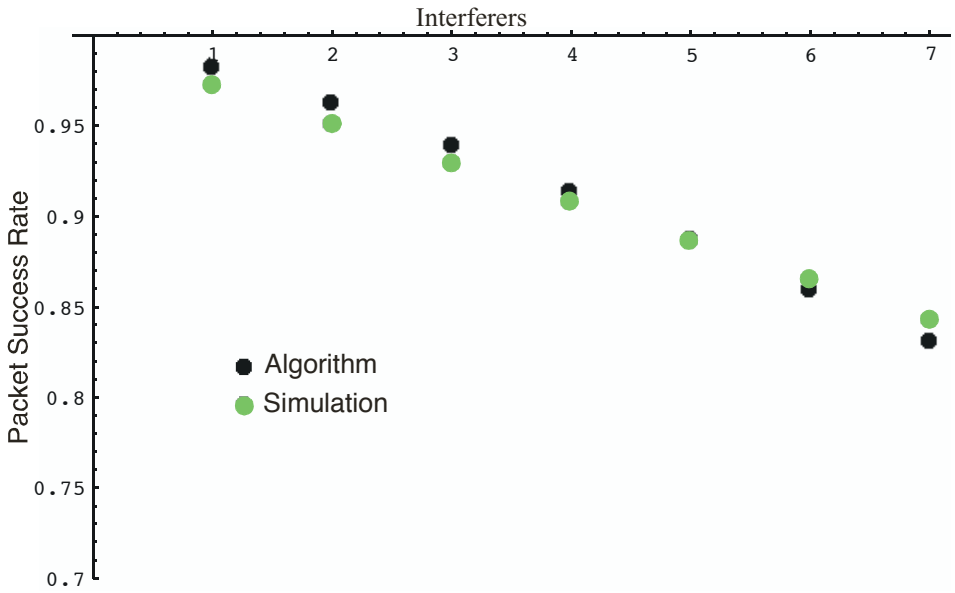

Figure 5.2: Frame success rate comparison of the algorithm solution with a simulation with a varying numbers of interfering sources with identical characteristics.

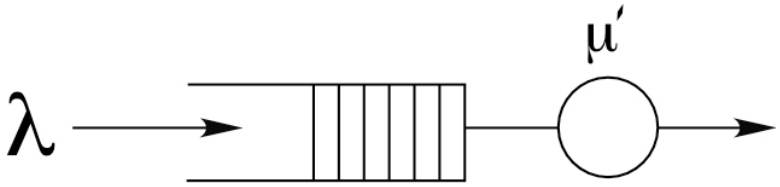

Figure 5.3: Effective $M|D|1$ Queue capacity for variable rate UWB channel defined as μ'

of bursty packet interference. All interfering packet lengths were fixed at 4 ms producing a pulse frame rate $T_f = 10$ ns. This represents a stressing high pulse blanking density that an adaptive link would be forced to cope with. Each interferer, for this example, generated packets at a rate of $\lambda = 30$ per second. The adaptive rate link used a frame rate of $T_f = 100$ ns with varying chip rates of from 3 to 8 chips per bit. The packet data size is fixed at 5000 bits for a maximum packet length of 4 ms. The frame success rate was determined by the algorithm using optimized rate tables (5.1) for various numbers of interferers. The same case is compared to a simulation in Fig. 5.2 and show good agreement with less than than a 1% deviation with up to seven stressing interferers.

Using the predicted frame failure rate and the chip per bit rate selected in the algorithm, the optimum rate table is found that maximizes the effective throughput of the transmit

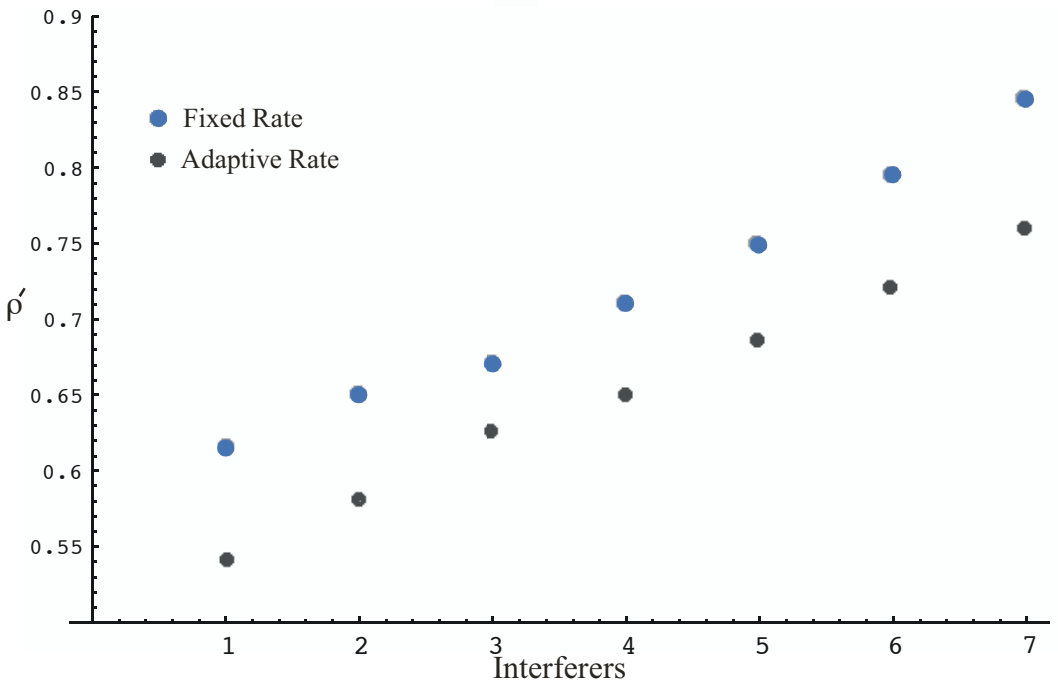

Figure 5.4: Equivalent $M|D|1$ queue throughput for optimized adaptive rate UWB and a fixed rate 5 chip/bit link.

queue. Because of the adaptive pulse rate used in this UWB technique, the effective channel capacity is not constant. By using queue loading statistics, as in [38], we can equate these loading averages to a theoretical $M|D|1$ queue [52] of capacity μ' as shown in figure 5.3. For each of the interfering cases optimized above, the effective throughput as defined by

$$\rho' = \frac{\lambda}{\mu'} \tag{5.20}$$

was equated to the queue loading statistics from the simulation and plotted in Fig. 5.4. Estimating the optimum rate table with simulation of queue throughput is a slow process but showed the derived solutions with the algorithm to be accurate.

To illustrate the advantage of adaptive pulse rate control, the same throughput performance was compared to a fixed rate system. For the cases considered, the best overall average fixed pulse rate was found to be 5 chips per bit with its effective throughput plotted along with the optimized adaptive rate performance in Fig. 5.4. In all cases the adaptive

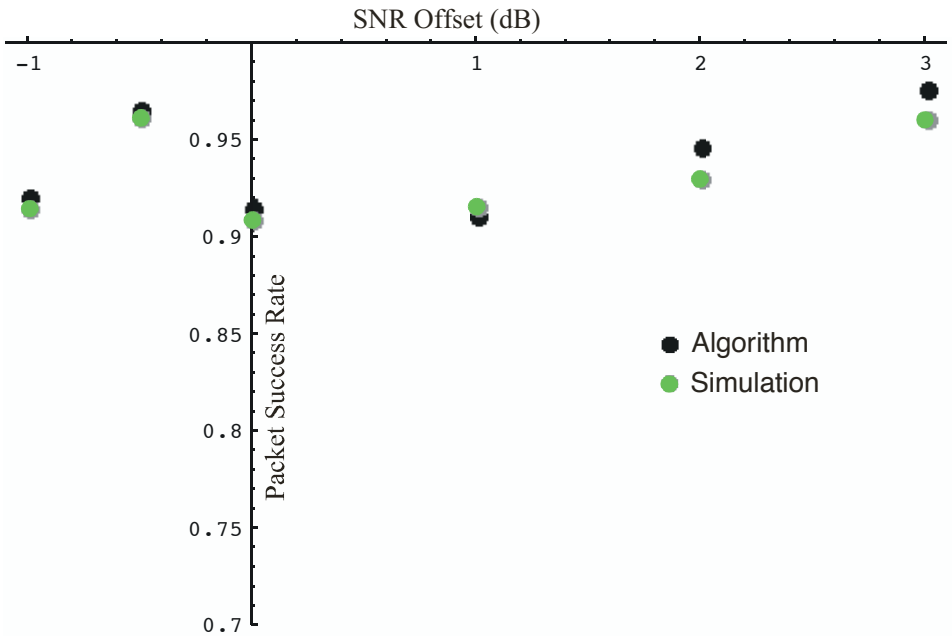

Figure 5.5: Packet success rate with 4 interfering sources within a range of quiescent background SNR values.

rate system took advantage of relatively quiescent periods to decrease the needed pulse rate and reduce the transmission time of the packet.

The algorithm is also used for performance evaluation of other parametric variables such as background SNR, pulse width, and frame rates. The packet success rate for four interfering sources over a range of quiescent background SNR values is compared in Fig. 5.5 with simulation. The relative reference point defined as 0 dB here, is the operational SNR used in Fig. 5.2 with the packet success criteria set at a BER $\leq 10^{-3}$. Although the packet success rate here is not monotonic with SNR as one would normally expect, the rate control table was optimized in each case for packet throughput. This optimization trades packet success performance for transmission time to effect the best throughput performance which is not always commiserate with improved packet success.

The relative pulse frame times or pulse widths can be parametrically evaluated in the algorithm. An example of the same four interferer case is considered where the pulse width is varied around the nominal 1.2 ns in Fig. 5.6. Again the rate table is optimized for channel throughput at each point and results in trades between packet success and duration.

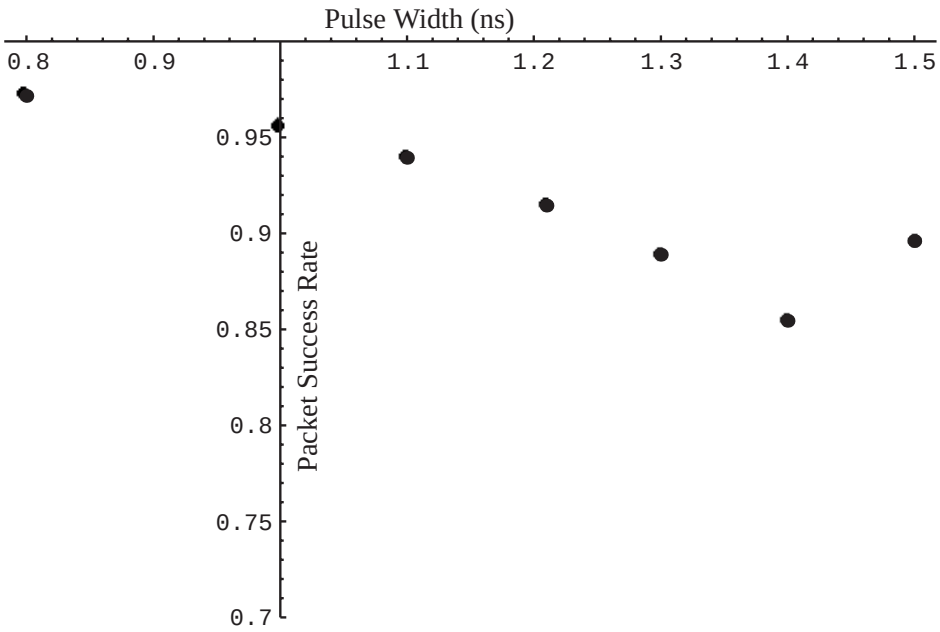

Figure 5.6: Probability of packet success with optimized rate tables over a range of varying pulse widths.

The average number of chips per bit used at each pulse width is also shown in Fig. 5.7. The improvement in packet success for the larger pulse width is marked by the rate table adjustment to provide more bit error immunity and extended packet duration.

5.3 Conclusions

This chapter develops a theoretical basis for packet transmission success using adaptive chipping (spreading) rates under harsh near-far power ratio environments. Motivated by the uncertain dynamic range of tactical environments, the method leverages the low duty cycle characteristic of impulse radio to mitigate the effects of powerful interferers by selective pulse blanking. The theory is used to develop the best spreading rates required to optimize packet throughput performance for fixed size data packets. Packet duration is in turn dependent on the selected spreading rate witch is conditioned on the level of interference detected. Simulation results show good agreement with theoretical solutions of packet suc-

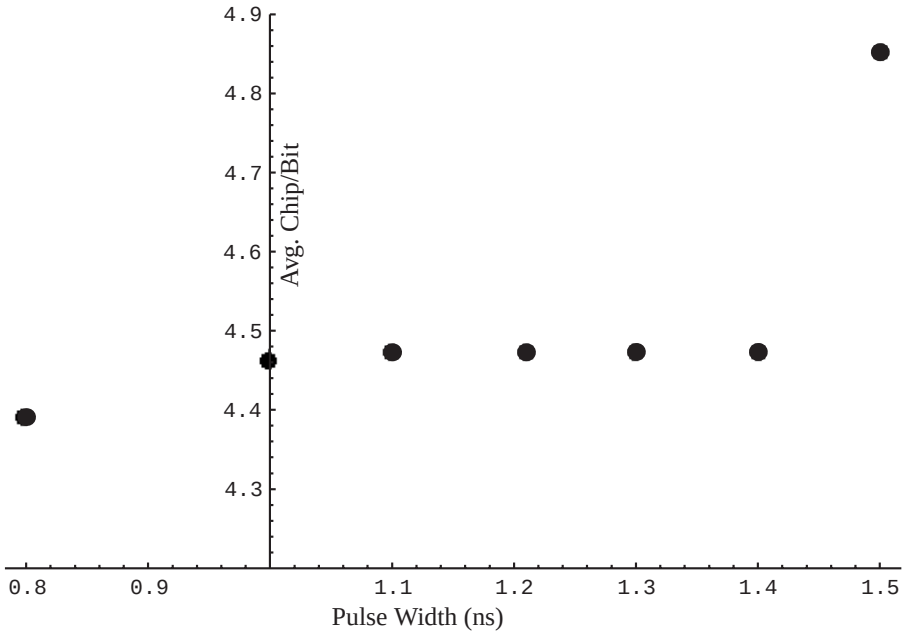

Figure 5.7: Average chip/ bit rate required with an optimized rate table over a range of variable pulse widths.

cess probabilities. The combination of adaptive rate techniques with optimized rate tables are used to illustrate the throughput efficiency over fixed rate methods.

Chapter 6

ALOHA Capacity with Perfect Blanking

The high multi-user density supported by UWB with its low duty cycle transmissions makes it an attractive candidate for independent autonomous networks. Point-to-point packet systems based on slotted [58] and un-slotted ALOHA protocols have been suggested for CDMA [59, 60, 61]. Many narrow band analyses of such systems have assumed packet failure for any partial packet overlap. Analysis applied to CDMA [40] have tried to determine the packet success rates for all partial overlap cases given the survivability of spread spectrum systems in mutual interference.

Although most cases presented for CDMA are based on high SNR equal power assumptions the potential throughput supported by UWB under these same conditions is quite large. UWB, however, will significantly degrade performance under conditions of unequal power. We have presented techniques [36, 37] that allow for autonomous discrimination in large near far power conditions that can be applied to uncoordinated networks. In this chapter we adapt the techniques described in [40] to determine UWB performance under high SNR conditions with very harsh power disparity using chip discrimination and hard limiting techniques from [36, 37]. Pulse collisions are assumed mitigated by chip discrimination or hard limiting techniques with the surviving pulses applied to the bit decision sum. This case represents a worst case analysis for a dense population of transponders. To make best use of Impulse Radio's (IR) multi-user independence a simple ALOHA proto-

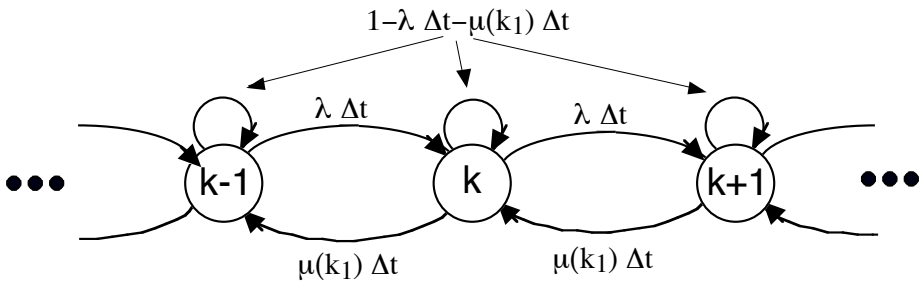

Figure 6.1: Markov state transition probabilities

col is used and later modified to include the equivalent of a Channel Load Sense Protocol (CLSP). Initial cases using assumed known interference densities at the beginning of the packet is later modified to estimate this interference level with the use of self derived chip level exceedance counts. In addition to fixed chip rates we apply the derived interference levels to an adaptive rate control technique to achieve near optimum system throughput with a substantial reduction in overall pulse density.

6.1 System Model

The method described in [40] models the probability of transition from k interferers at each bit in a packet as a Markov process. The transition probabilities shown in Fig 6.1 assume an equal length packet Poisson arrival rate of λ packets/sec and a departure rate $\mu(k_1)$ determined by the number of interfering packets at bit 1.

The expression from [40] for packet success probability up to the i^{th} bit is shown again here as:

$$\begin{aligned} P_s(k,i,k_1) = \; & P_s(k,i-1,k_1)(1-\mu(k_1)\Delta t-\lambda\Delta t)(1-\varepsilon_\kappa(k)) \\ & +P_s(k+1,i-1,k_1)\mu(k_1)\Delta t(1-\varepsilon_\kappa(k+1)) \\ & +P_s(k-1,i-1,k_1)\mu(k_1)\lambda\Delta t(1-\varepsilon_\kappa(k-1)) \end{aligned} \tag{6.1}$$

where $\varepsilon_\kappa(k)$ is the probability of symbol error given k interferers. The resulting packet error is the double sum over all k and k_1 cases for a packet of length L bits is given by:

$$Q_s = \sum_{k=0}^{\infty} \sum_{k_1=0}^{\infty} P_s(k, L, k_1)(1 - \varepsilon_\kappa(k)) \tag{6.2}$$

The validity of this method assumes only the single transition from k to $k \pm 1$ and thus the constraint on the transition rates.

$$\begin{aligned} \lambda\, \Delta t &<< 1 \\ \mu(k_1)\, \Delta t &<< 1 \end{aligned} \tag{6.3}$$

The numerical stability and computational complexity of this technique must be carefully considered. Packets with large bit counts can become a problem for some packet densities. We have modified the technique in [40] to accommodate larger packet sizes by partitioning the packet into κ bit symbols, remaining mindful of the constraints required by (6.3) for symbol periods of Δt. The resulting symbol success rate used in (6.1) for κ bits will be:

$$\varepsilon_\kappa(k) = 1 - (1 - \varepsilon_b(k))^\kappa \tag{6.4}$$

Our evaluation of UWB assumes an un-slotted ALOHA network. The packets are all of equal length with the same number of pulses per bit. The SNR relative to thermal noise is assumed high. In the case of the hard limiter, pulse collisions are assumed to result in random error from the individual chip contribution to the decision sum. Under these assumptions the bit error probability of a hard limiter for n chips/bit and k interferers is

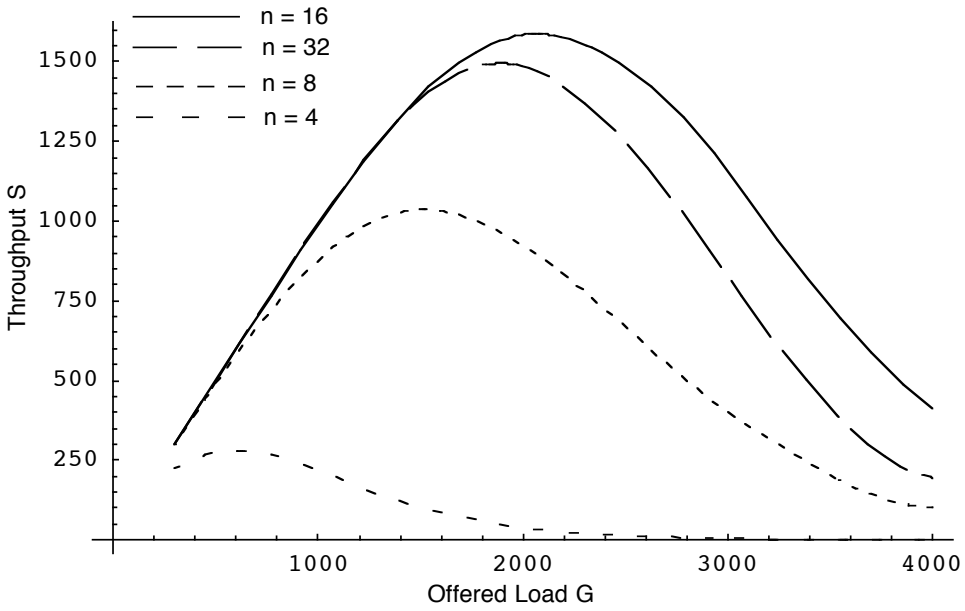

Figure 6.2: System throughput for a high SNR hard limited UWB un-slotted ALOHA packet network. Packet duration 4 ms.

given by:

$$\varepsilon_b(k) = \begin{cases} \sum_{i=0}^{\frac{n}{2}-l-1} \binom{n-l}{i} \left(\frac{1}{2}\right)^{n-1} + \frac{1}{2}\binom{n-l}{\frac{n}{2}-1}\left(\frac{1}{2}\right)^{n-1} \\ \qquad\qquad \text{if } \{n \Rightarrow Even \ , \ l \leq \frac{n}{2}\} \\ \sum_{i=0}^{\lceil \frac{n}{2} \rceil - l-1} \binom{n-l}{i} \left(\frac{1}{2}\right)^{n-1} \\ \qquad\qquad \text{if } \{n \Rightarrow Odd \ , \ l \leq \frac{n}{2}\} \\ 0 \qquad\qquad Otherwise \end{cases} \tag{6.5}$$

We now use (6.2) and (6.5) to determine the system throughput for a fixed duration packet of 4 ms and L = 5000 bits. The binary offset pulse correlation width is 1.2 ns. The throughput is defined as

$$S = G\, Q_s \tag{6.6}$$

where G is the Poisson offered load in packets per second [62]. The throughput will vary depending on the chip rate and adjusted chip frame time T_f required to maintain the packet duration of 4 ms. Fig. 6.2 compares the throughput for varying chip rates. A peak throughput of 1600 packets per second is obtained with a $n = 16$ chip per bit rate.

The same analysis can be applied to the chip discrimination technique described in [36] where in this case we assume perfect blanking of interfering pulses. The bit error rate for k interferers under the same assumptions above is given by

$$\varepsilon_b(k) = \sum_{i=0}^{n} \binom{n}{i} (1-\gamma)^{xi} (1-(1-\gamma)^x)^{n-i} \frac{1}{2} \operatorname{Erfc}\left[\sqrt{i\frac{s_c}{2\sigma_c^2}}\right] \tag{6.7}$$

where n is the number of chips per bit and γ is the ratio of the pulse correlation widow width to the chip frame time T_f.

Evaluation of (6.7) with (6.2) and a fixed packet duration of 4 ms is also compared in Fig. 6.3. Again the peak throughput is achieved with a chip per bit rate of $n = 16$ at nearly 7000 packets per second. This is a worst case scenario since all pulses in the environment are assumed potential blanking pulses. Simulation values for $n = 16$ are plotted with theoretical values in Fig. 6.3 and are in good agreement.

The same technique can be applied to a Channel Load Sense Protocol (CLSP) as described in [40]. When packet density is limited to α concurrent packets, the Markov state transition is limited to $\alpha - 1$ as shown in Fig. 6.4. Modifying the expressions in (6.1) and (6.2) to that of a $M|D|\alpha|\alpha$ queuing system and applying the same IR bit error expressions, the optimum capacity limit α can be easily assessed. Using the same packet parameters from Fig. 6.3 ($T_f = 25$ ns) the optimum load limit was found to be $\alpha = 17$ with the resulting system throughput illustrated in Fig. 6.5. For the same packet size of 5000 bits the pulse frame time T_f was varied from 10 ns to 100 ns. Despite the corresponding increase in packet duration with T_f, performance improves for the 100 ns case. The stochastic nature of pulse collisions for increased pulse frame time is a greater influence on performance than increased packet collision rates but with diminishing returns over the 25 ns sample case.

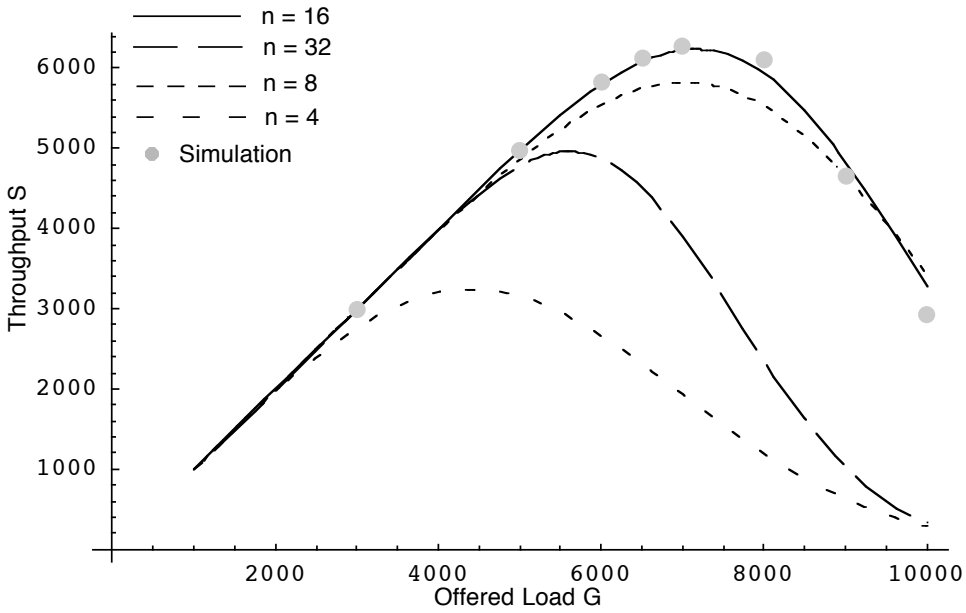

Figure 6.3: System throughput for a high SNR un-slotted ALOHA packet network with perfect blanking chip discrimination. Packet duration = 4 ms.

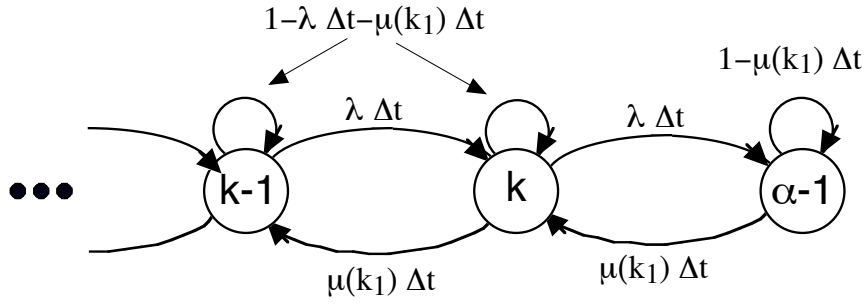

Figure 6.4: Markov state transition probabilities for CLSP

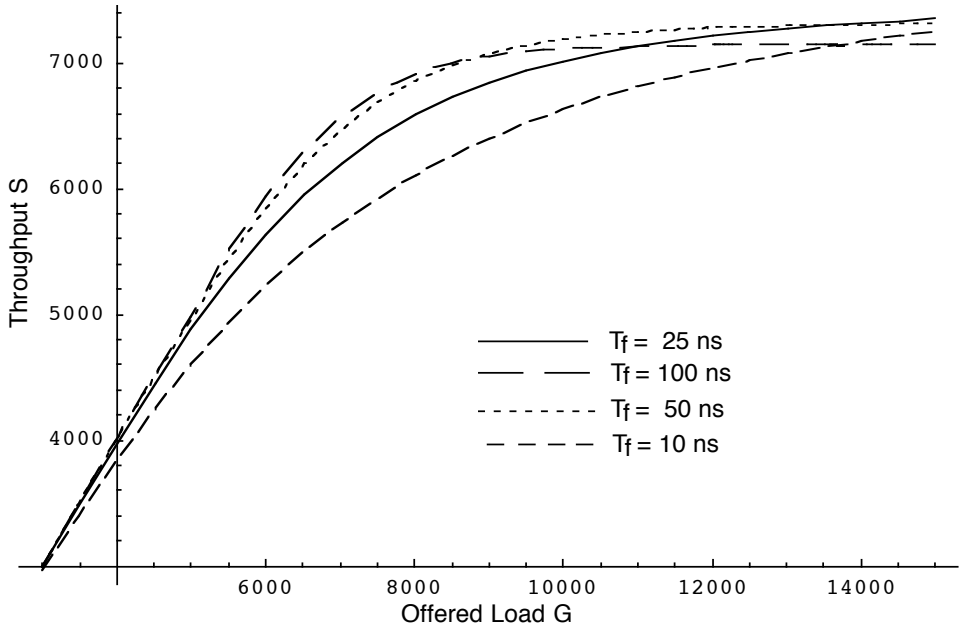

Figure 6.5: High SNR chip discrimination using CLSP optimal at $\alpha = 17$ for $C_b = 16$ and varying pulse frame times.

6.2 Simulation

The theoretical method and cases considered thus far are limited to identical packet duration and chip per bit rates. A technique for adaptive rate UWB packet transmission was presented in [38] and is interesting to compare to the un-slotted ALOHA fixed rate methods. The simulation used for validation in section 6.1 is modified to select an appropriate chip per bit rate based on the number of known interfering packets k_1.

The same pulse width was selected for these cases with the chip frame time fixed at $T_f = 25$ ns. The selected rate table used for this case is described by Fig. 6.6. Note that the table is limited to 16 interferers. Arriving packets in excess of this limit are not transmitted and assumed lost, effectively implementing a CLSP limit of $\alpha = 17$.

Simulations and theoretical solutions of the optimum fixed chip per bit rate un-slotted ALOHA throughout are compared in Fig. 6.7. The optimum fixed chipping rate was found to be $n = 16$ with an optimum CLSP limit of $\alpha = 17$. The adaptive rate method based on Fig. 6.6 was found to be very close to this system throughput with one very important difference. The network pulse density comparison in Fig. 6.8 shows a substantial reduction

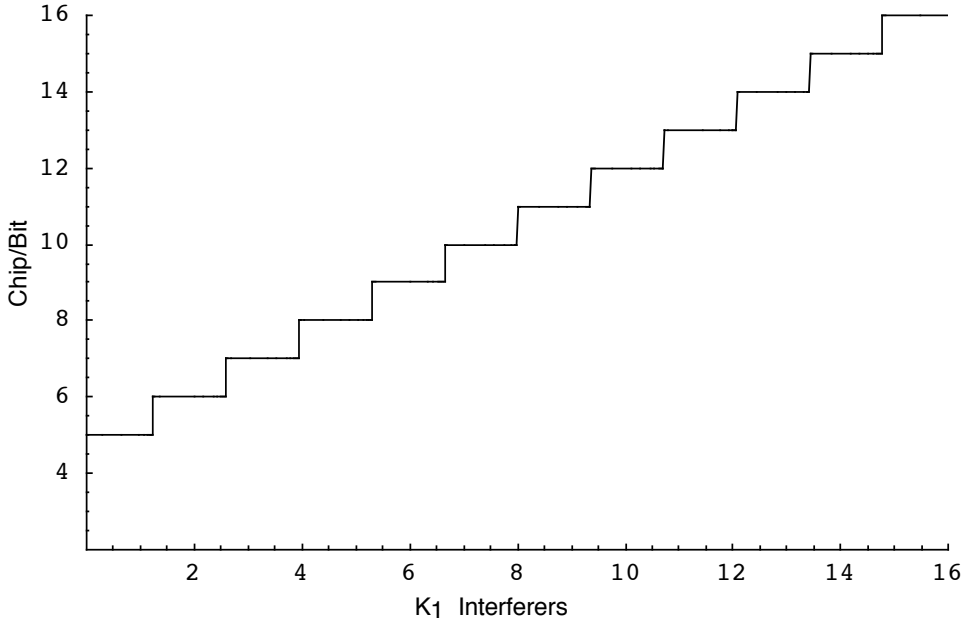

Figure 6.6: Variable chip per bit rate table used for k_1 known interfering packets.

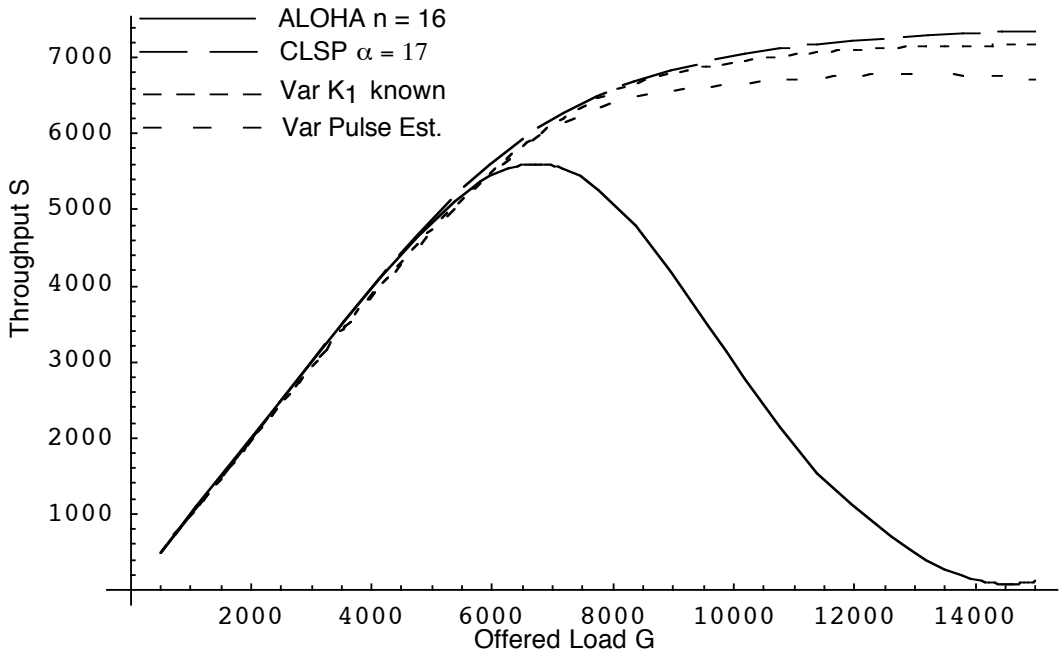

Figure 6.7: Throughput comparisons of fixed $n = 16$, $\alpha = 17$ CLSP and adaptive rate methods.

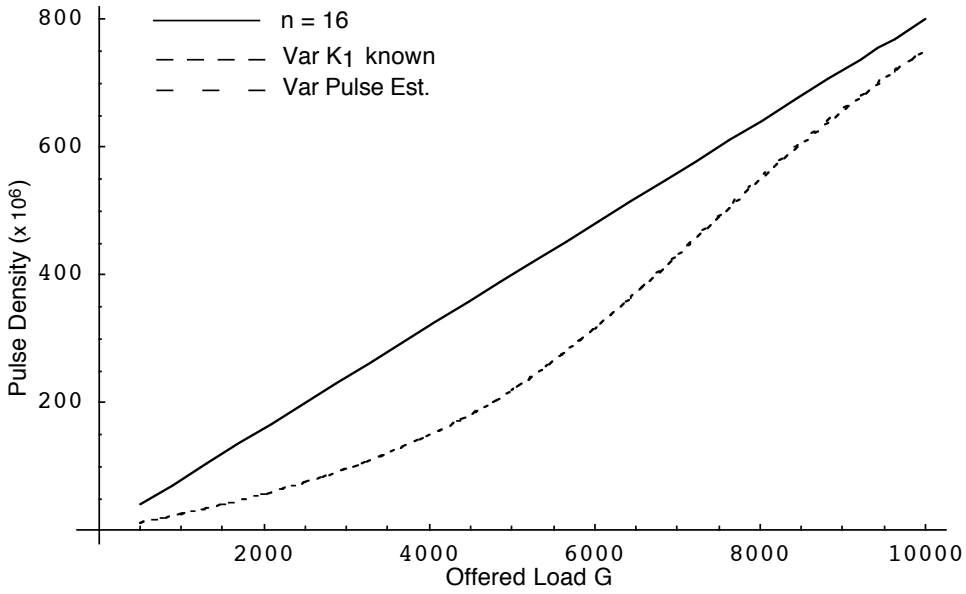

Figure 6.8: Channel pulse density for a given offered load.

in the required pulses needed to effectively meet the same system throughput. To better understand the reduced pulse density, the decline in number for the adaptive rate method as a percentage over that of the fixed 16 chip per bit method is shown in Fig. 6.9. The variable rate method effectively adapts to the offered load with the minimum number of pulses required to achieve throughput. In effect using the minimum signal power required for transmission.

The implementation of this adaptive rate method up to this point has been based on an assumed known number of interferers k_1 at the origination of each packet. A potentially impractical assumption even for narrowband systems. An autonomous method of estimating the interference level introduced in [38, 36] however can be used with IR. In this implementation the receiver opens it's pulse receiver at the nominal frame rate $T_f = 25$ ns over a period of $125\mu s$ just as it would for nominal reception as illustrated in Fig. 6.10. However, rather than detecting PPM chips for IR data, each reception is compared to an exceedance threshold. The number of detection exceedances out of these 5000 samples can be used to estimate k_1. This pulse exceedance count can be used as part of a simple point-to-point MAC layer protocol to select the most efficient chip per bit rate given the conditions.

The equivalent rate control table in Fig. 6.11 now maps the pulse exceedance count to

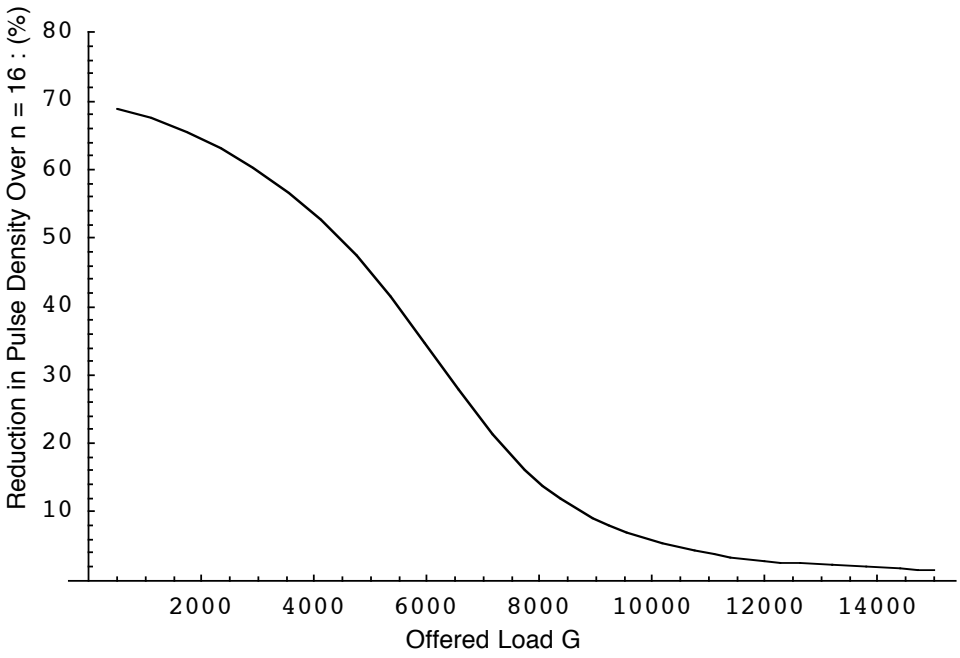

Figure 6.9: The reduction in pulse density as a percentage over the fixed $n = 16$ case.

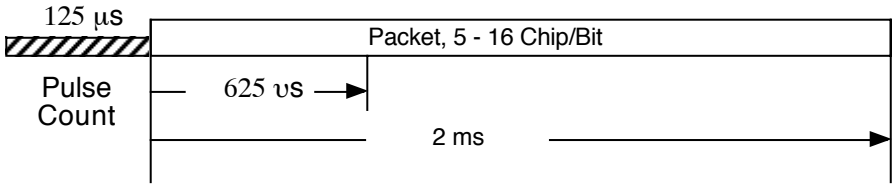

Figure 6.10: Packet Frame Timing

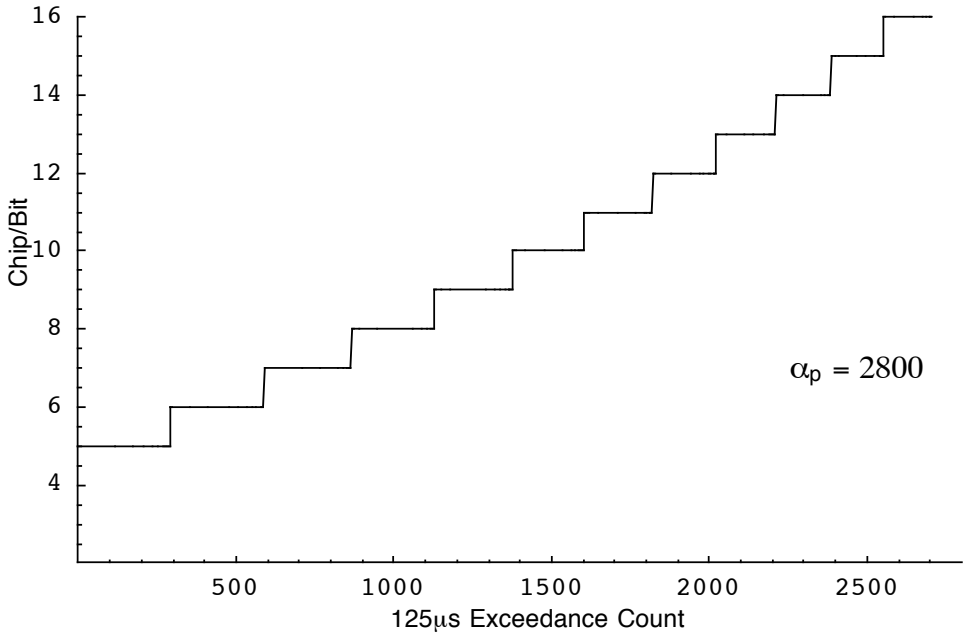

Figure 6.11: Pulse exceedance count rate table

the appropriate chip per bit rate. Some reasonable implementation error associated with an exceedance count variance would be expected. The network throughput as compared to the previous cases in Fig 6.7 shows only a slight implementation loss with this simple estimator. The effective pulse density reduction is indistinguishable from the known k_1 interferer case in Fig. 6.8.

Not only can we dynamically adapt the power required for packet transmission we do so nearly achieving the optimum capacity of the best fixed rate system. All the information required to determine the needed chip per bit rate can be easily obtained with locally derived information without special modification of the receiver.

6.3 Conclusion

This chapter has adapted techniques developed for un-slotted ALOHA CDMA packet error estimation to Impulse Radio with pulse blanking. The method estimates the probabilities of k interferers arriving at each bit in the packet as a Markov process. Using this tech-

nique with expressions for a hard limited impulse receiver as well as chip discrimination with assumed high SNR relative to thermal noise we show anticipated system throughput. We show that the peak capacity is also dependent on the number of chips per bit used. Theoretical results are in very good agreement with simulation over a broad offered load.

This theoretical technique is also applied to a CLSP protocol optimizing IR throughput for the chip rate n as well as the limit parameter α. Since the CLSP technique applied to ALOHA is similar to adaptive rate tables described in Chapter 4 we compare simulations to the best fixed chip rate case. Not only does the adaptive rate IR technique approach the best fixed rate capacity, it does so with a substantial reduction in the required pulse density, interference and required power. Theoretical results based on an assumed known number of interferers at the beginning of packet transmission showed performance consistent with simulations deriving this interference from passive pulse counts. The results here have shown how chip discrimination and rate control can be applied to simple packet protocols for effective packet protection from near-far power disparity with self derived estimates of interference.

Chapter 7

Conclusions

As a relatively novel communication technology, academia and industry have both made strides in developing UWB as a potential solution for local area networks. Such momentum for UWB has even motivated the FCC to make special spectral allocations available to UWB for early testing. Theoretically UWB has shown substantial potential for high throughput in dense muti-user networks but many limitations remained to be addressed. In this dissertation, we have advanced the understanding of two of the more critical performance issues confronting UWB. We find it important to develop a fundamental understanding of the limiting performance issues of IR before applying complex network protocols derived from long accepted narrowband technologies.

The time domain nature of UWB and inherent stringent timing constraints, addressed first in Chapter 2, quantified the timing jitter tolerances required to maintain widely acknowledged IR performance expectations. Clock jitter is a relatively minor parametric consideration in most narrowband systems but can significantly degrade UWB performance. We quantified the timing jitter tolerances required to maintain widely acknowledged IR performance expectations and were the first to introduce the issue in [13, 14]. Not only is the tolerance of the clock a design consideration but the potential effects of practical tracking present additional timing errors. We initially developed a conventional Early-Late gate tracking method adapted to UWB to illustrate the additional link jitter at operational signal

levels. This method added as much as 10 ps RMS to the timing jitter budget and proved to be an awkward implementation for UWB.

Applying careful consideration to the unique time domain requirements and the nature of the relatively wide inter-pulse spacing argues against narrowband techniques. Based on this we developed an error tracking architecture derived from ML methods. Not only is the complexity significantly reduced over the Early-Late Gate approach but the performance provides further insight into potential independent tracking channels and network timing. In addition to the timing effects on decoding performance we address another important design consideration by quantifying the mean time to lost lock for the loop. This is an important consideration given the potentially long time required to (re)acquire link timing in UWB. The simulation results show good tracking stability for non data assisted links with a first order narrow band loop filter. Clock offsets equivalent to a 100 mph offset velocity can be tracked with 2dB loss in the decoding SNR. Data assisted tracking is primarily limited to the decoding SNR performance. The results show how closely coupled the tracking performance is to the overall design of an IR link. This architecture also suggests a network concept of low power independent timing channels supporting higher power data transmissions. More importantly the low power timing channel would allow for low latency transmission when timing acquisition would be prohibitive.

Much of the anticipated performance described in the literature to date is also based on ideal equal power assumptions. Just like the considerations for timing in Chapter 2, the practical issues of power inequality are addressed in Chapter 3. Here we have undertaken the commonly acknowledged IR multi-user interference problem with a unique and simple chip discrimination technique [36, 37]. We show how traditional matched filter implementations of IR can be modified to adapt to large near-far pulse interference levels to maintain performance. Not only does this technique allow for sustained links where previous methods completely deteriorate, but uses autonomous self derived information to sense the level of interference and set thresholds. By taking advantage of the excess bandwidth often available to UWB, we can use it to mitigate a realizable damaging power disparity. The proposed method addresses potential pulse interference issues associated with uncooperative tactical environments, potential multi-path co-site network arrangements, and even self interference.

Unlike some narrowband techniques, measuring the level of interference in UWB is more difficult than simply integrating power in the channel. The very advantage of the low duty cycle nature of UWB is the ability to limit the operation of the receiver. The chip discrimination technique however suggests an efficient way of passively estimating the degree of interference at the receiver without unduly increasing the receiver duty cycle. Leveraging the discrimination logic in our architecture and incorporating a circular counter provides an efficient and simple estimate of interference. This combination is utilized in Chapter 4 to adapt to dynamic levels of pulse interference. The estimate of interference can be used to select the appropriate IR spreading rate and optimize the throughput of a packet queue. Simulations of a simple peer-to-peer MAC layer protocol were constructed demonstrating the throughput advantages over commonly implemented fixed parameter systems [38].

The simulation results have been corroborated with theoretical estimates in Chapter 5. Developed for harsh interfering cases, this model was derived assuming perfect blanking and maintained close agreement with practical discrimination techniques described in Chapter 4. The algorithm has been shown useful as a rapid development tool for determining the best spreading rates required to optimize packet throughput performance for fixed size packets. Results here are useful in describing the effects of arbitrarily defined interference environments on IR packet transmissions. The theory is extended in Chapter 6 to address the overall network performance.

We gain insight into the effects on network performance when the adaptive techniques developed thus far are applied to a simple ALOHA network in Chapter 6. This was accomplished by using Markov process techniques derived for ALHOA CDMA networks and adapting it to UWB. Again focusing on the harsh power disparity environment we show optimum system throughput for varying spreading rates and frame durations. For a select packet duration and frame rate, the spreading rate required to optimize system throughput is derived. When the adaptive rate techniques are applied to all members of the network, the throughput performance is much like a conventional CLSP ALOHA network with one important difference. We approach the theoretically predicted optimum capacity with a significant reduction in pulse density.

We have specifically addressed some of the more pressing UWB multi-user perfor-

mance issues by leveraging the unique characteristics of impulse radio. Not only have we adapted methods to mitigate these issues but have accomplished it with a low degree of complexity. We have shown that adapting accepted narrowband methods to UWB requires a better understanding of the fundamentals of UWB.

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